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Article

Energy Efficient Tri-State CNFET Ternary Logic Gates

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Abstract: Traditional silicon binary circuits continue to face challenges such as high leakage power dissipation and large area of interconnections. Multiple-Valued Logic (MVL) and nano-devices are two feasible solutions to overcome these problems. In this paper, we present a novel method to design ternary logic circuits based on Carbon Nanotube Field Effect Transistors (CNFETs). The proposed designs use the unique properties of CNFETs, e.g., adjusting the Carbon Nanotube (CNT) diameters to have the desired threshold voltage and have the same mobility of P-FET and N-FET transistors. Each of our designed logic circuits implements a logic function and its complementary via a control signal. Also, these circuits have a high impedance state which saves power while the circuits are not in use. We show a more detailed application of our approach by designing a two-digit adder-subtractor circuit. We simulate the proposed ternary circuits using HSPICE via standard 32nm CNFET technology. The simulation results indicate the correct operation of the designs under different process, voltage and temperature (PVT) variations. Moreover, we designed a two-digit adder/subtractor and a power efficient ternary logic ALU based on the proposed gates. Simulation results show that the two-digit adder/subtractor using our proposed gates has 12X and 5X lower power consumption and PDP (power delay product) respectively, compared to previous designs.

Keywords: Multiple Valued Logic (MVL); CNFET; Energy-Efficiency; Nano-electronics; Ternary Logic, Adder, ALU

1. Introduction

Conventional silicon binary computing faces significant problems in terms of power and performance. Some of the most important challenges are the severe short channel effects of the Si-MOSFET and the restriction in the number of wires and pins of the chips that play more important roles than the device geometry. To overcome these challenges, one solution is to utilize non-silicon and non-binary circuits [1].

In order to use non-binary computing, the MVL paradigm has been introduced as an alternative to binary computing. In MVL, more than two logic values are used for data representation. More information can be conveyed over the same line and more data can be stored per memory cell by utilizing MVL techniques [1]. Also, using more than two significant logic levels leads to fewer computational steps, potentially fewer gates and considerable reduction in the number of interconnections and pins [2-4]. It was proven that e base (e ≈ 2.718) leads to the most efficient implementation of the switching systems among all MVL systems [2]. Therefore, ternary logic is superior to binary logic since three is the closest integer to e. Ternary logic provides the most

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efficiency with its lower energy consumption, as a result of the reduction in the number of interconnection wires and the cost of data movement.

In nanoscale CMOS devices leakage power is an important part of its total energy consumption. Other critical challenges are the reduced gate control and velocity saturation [5]. Therefore, to continue the historical improvement in chip transistor count, density and performance while operating at low-power, some emerging devices and technologies have attracted considerable attention in the recent years as alternatives for CMOS, such as quantum dot cellular automata (QCA), carbon nanotube field effect transistor (CNFET), single electron transistor (SET), nano magnetic devices, *etc.* [6-8]. Among these new technologies, CNFETs have attracted a lot of attention as a potential successor for CMOS because of its outstanding characteristics such as similarities with MOSFET, high carrier mobility, high I_{ON}/I_{OFF} ratio, unique one dimensional band structure and near ballistic transportation [9, 10].

CNFET transistors are even more interesting, when they are used in designing MVL circuits. MVL circuit design is based on multiple threshold design techniques and adjusting the threshold voltage of CNFETs is easily possible by changing the diameter of the nanotubes [11,12]. In recent years, some MOSFET and CNFET MVL circuits, have been presented for ternary and quaternary logic [10,11,13-21]. However, they have some critical drawbacks such as using very large ohmic resistors [13,14], requiring obsolete depletion-mode MOSFET [15,17-20], non-full swing nodes and limited fan-out [21]. In this paper, we propose a novel method for designing ternary logic gates Buffer/NOT, AND/NAND, and OR/NOR. Each of the designs produces a logic function with its complimentary by a control signal. Moreover, a third state of high impedance is introduced to achieve power efficiency if none of the two possible gates is needed.

This paper extends the contributions of [22], in which ternary basic gates based on CNTFETs were introduced. In this current paper, we make additional contributions by presenting a two-digit adder/subtractor as an application for the proposed basic gates in addition to detailed analysis with several figures of merit, such as propagation delay, power dissipation and the power-delay product (PDP). In addition, a low power ternary arithmetic logic unit (ALU) based on the presented circuits is designed and analyzed.

The rest of this article is organized as follows: Section II briefly reviews some background on CNFET devices and ternary logic. Section III describes the proposed designs. Section IV presents the simulation results and analyses. Finally, section V concludes the article.

2. Background

2.1 Carbon Nanotube Field Effect Transistor

A carbon nanotube (CNT) is a sheet of graphene rolled up along a chirality vector [23]. The chirality vector of a CNT is defined by (n, m) pair. If n-m = 3k ($k \in Z$) where Z is the set of integer numbers, then the CNT behaves like a metal, otherwise like a semiconductor [12].

Metallic nanotubes are attractive as future interconnects because of their superior properties, such as large current carrying capacity, and high thermal conductivity [24]. Also semiconducting nanotubes have great advantages. They can be used as channels in field effect transistors. They have high charge carrier mobility, lower sub-threshold swing and fewer parasitic elements [3]. Moreover, they are very attractive to the Silicon semiconductor industry for the following reasons:
(1) The operation principle and the device structure are similar to CMOS devices; therefore, we can reuse the CMOS fabrication process and established CMOS design infrastructure. (2) CNFETs show significant improvements in device performance metrics such as delay and power consumption in experimental results [25].

This three (or four) terminal device (CNFET) is turned on or off electrostatically via the gate and its threshold voltage (V_{th}). One of the most effective properties of CNFET, which makes it very suitable for designing digital circuits, is that the desired threshold voltage can be obtained by choosing the proper diameter for the CNT. The threshold voltage of a CNFET is given by the following equations, where, e is the unit electron charge, E_{bg} is the CNT bandgap, a_0 ($\approx$0.142 nm) is

the carbon to carbon bond length in a CNT and V_π (≈3.033 eV) is the carbon π-π bond energy in the tight bonding model [26].

(1)

$$V_{th} \approx \frac{E_{bg}}{2e} = \frac{a_0 E_\pi}{eD_{CNT}} \approx \frac{0.436}{D_{CNT}(\text{nm})} \quad (1)$$

$$D_{CNT} = \frac{\sqrt{3}a_0\sqrt{n^2+m^2+nm}}{\pi} \approx 0.0783\sqrt{n^2+m^2+nm} \quad (2)$$

According to Equation (2), the threshold voltage of a CNFET is inversely proportional to the CNT diameter.

Although CNFETs are promising, there are several challenges that need to be addressed. There are some difficulties for synthesis or growth of nanotubes with identical diameters and chiralities. Changes in tubes' diameter and wrapping angle, defined by the chirality indices (n, m), will shift the electrical conductivity and CNFET threshold voltage. However, many effective and feasible solutions have already been presented in the literature for growing CNTs with a specific chirality and setting the desired threshold voltage [27, 28]. Moreover, it is difficult to control the exact placement and alignment of CNTs at a VLSI scale. Mispositioned CNTs may cause incorrect logic functionality [29,30].

2.2. Ternary Logic

Ternary logic consists of three significant logic levels represented by "0", "1" and "2" symbols. These logic levels are commonly counterpart to Zero Volts, ½V_{DD} and V_{DD} voltage levels, respectively. The ternary basic logic operations, which are the building blocks of many other complex logical and arithmetic quaternary circuits, can be defined according to (3), (4) and (5).

$$X_i \in \{0,1,2\}$$

$$X_i + X_j = Max\{X_i, X_j\} \quad (3)$$

$$X_i \cdot X_j = Min\{X_i, X_j\} \quad (4)$$

$$\overline{X_i} = 2 - X_i \quad (5)$$

where, − denotes the arithmetic subtraction, the operations +, •, and $\overline{\ }$ are the OR, AND, and NOT in ternary logic, respectively [31].

Three different type of ternary gates can be designed for each function. As an example for ternary inverter three logic gates can be defined; Standard Ternary Inverter (STI), Positive Ternary Inverter (PTI), and Negative Ternary Inverter (NTI). The truth tables of these gates for ternary inverter are shown in Table 1.

Table 1. Truth Table of PTI, NTI and STI, where a is the input

a	PTI(a)	NTI(a)	STI(a)
0	2	2	2
1	2	0	1
2	0	0	0

2.3. Related Works

There exists in the literature state-of-the-art CNFET-based ternary circuits. Raychowdhury and Roy introduced a CNFET-based ternary design [1]. The design had large resistive loads. This is hard to implement and integrate with CNFETs and also causes performance degradation and wastes area and power. Another ternary design has been presented by Lin, Kim, and Lombardi [12]. They replaced the resistors used in [1] with P-CNFET active loads which led to less area overhead, larger noise margins and higher performance compared to the previous design.

Moaiyeri *et al.* [32] presented ternary logic circuits based on the complementary CNFET design style which uses three different threshold voltages. This design produces NTI, PTI and STI by a single circuit unlike previous designs. We adopt the design style of [32] throughout this paper.

3. Proposed design(s)

In this section, we introduce ternary logic gates, including ternary Buffer/NOT, ternary AND/NAND and ternary OR/NOR gates. The proposed designs use just two different diameters for their CNFETs. From Equations (1) and (2), the CNFETs should have 0.783 and 1.487 nm diameters, respectively. The chiral numbers should be (10, 0) and (19, 0), respectively. The threshold voltages ($|V_{th}|$) should be 0.557V and 0.293V, respectively. Moreover, in these designs we can produce a high impedance state, which is useful when any of the logic functions is not needed. This state consumes very lower power compared to the two other states which have static power dissipation. In summary, in this paper we propose a ternary family of logic circuits which can have three output states specified via a control signal.

3.1. Ternary Buffer/Inverter

The proposed ternary Buffer/NOT circuit is shown in Fig.1. This circuit can act as a buffer or an inverter for a ternary input using a control signal (S).

When the signal S = 0, the circuit acts as a ternary buffer. In this case, if IN = 0, both NTI and PTI nodes (shown in Fig. 1) will be V_{DD}, T5, T6 will be OFF and T3 and T4 will be ON, consequently, the output will be discharged to the ground through path 4. When IN = 2 (V_{DD}) the NTI and PTI nodes will be 0, and T1 and T2 will be ON and the output will charge to V_{DD} (path 3). When, IN = 1 ($\frac{1}{2}V_{DD}$), PTI and NTI are V_{DD} and 0 respectively and T1, T2, T3 and T4 will be ON. So with a resistive voltage division, the output will be $\frac{1}{2}V_{DD}$.

When S = 2 (V_{DD}), the circuit performs the NOT function. In this case, T1 and T2 are OFF and T5 and T6 are ON. Assume that IN=0, so STI and PTI will be V_{DD} and consequently the output will be V_{DD} through paths 1 and 2. For other inputs the output will be determined based on a resistive division.

Finally, when S=1 ($\frac{1}{2}V_{DD}$), the output will be high impedance (HiZ). In this case, T1, T4, T5 and T6 will be OFF because of their threshold voltages which are higher than $\frac{1}{2}V_{DD}$. Therefore, we do not have any path to the output. In this state, the circuit consumes very low power compared to the other states which consume static power. This state of the circuit is very useful in low power applications where no need for neither the buffer nor the inverter functionality continuously. The operation of this design is summarized in Table 2.

Figures 2 and 3 show the voltage transfer characteristic (VTC) curves of the presented ternary buffer and inverter receptively. These schematics verify the correct operation and steep curve in the transition region, which leads to low average static power consumption. We used PTI(s) and NTI(s) for controlling T4 and T5 to have lower OFF current and consequently lower power consumption.

3.2. Ternary AND/NAND – OR/NOR

Using the same design methodology for the ternary Buffer/NOT circuit, we design a new ternary AND/NAND and a new ternary OR/NOR. The operation principles of these two circuits are similar to the ternary Buffer/NOT gate.

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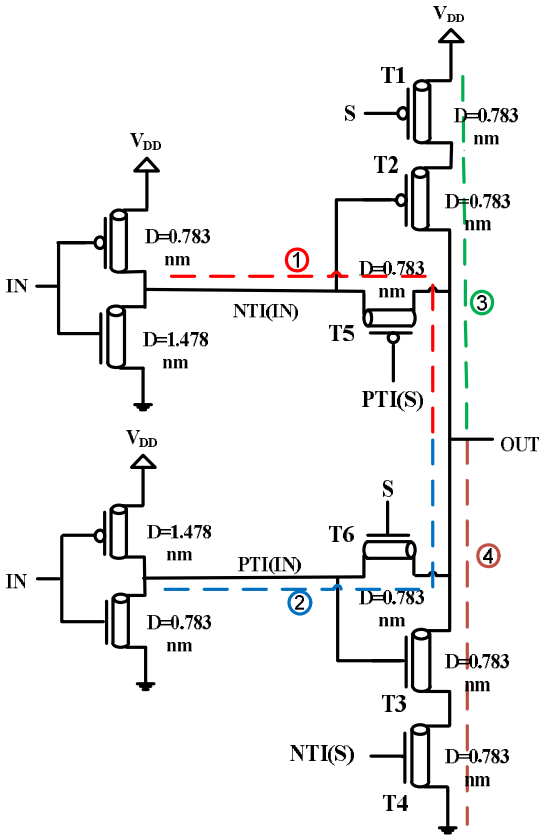
176

177 **Table 2.** Truth Table for the operation of the Buffer/NOT gate

S	IN	OUT
0	0	0
0	1	1
0	2	2
1	0	HiZ
1	1	HiZ
1	2	HiZ
2	0	2
2	1	1
2	2	0



178

179 **Figure 1.** The circuit design of our ternary Buffer/NOT Gate. This circuit has four different paths from
180 V_{DD} and ground to the output which are represented by numbers 1 -- 4. For each of the different inputs
181 two or three paths will be active.

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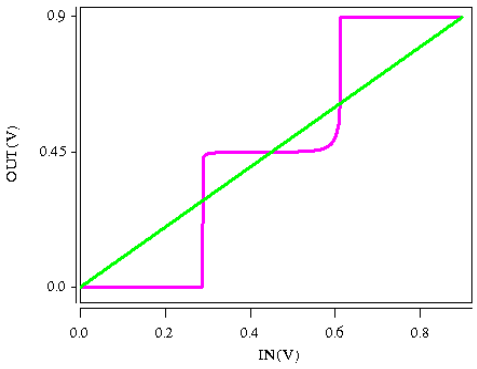

Figure 2. The Voltage Transfer Characteristic (VTC) of our proposed ternary Buffer

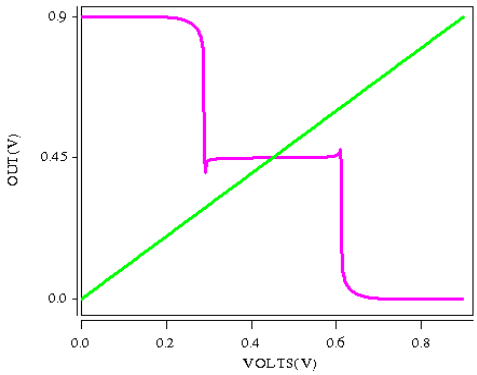

Figure 3. The Voltage Transfer Characteristic (VTC) of our proposed ternary Inverter

The schematics of the proposed AND/NAND and OR/NOR circuits are shown in Figs. 4 and 5, respectively. The operation of the ternary AND/NAND can be summarized as follows:

When both inputs (IN1, IN2) are around V_{DD} and S = 0, NTNAND and PTNAND nodes are discharged to ground, so the output will be V_{DD} through path 3. While one of the inputs is around $\frac{1}{2}V_{DD}$ and the other one is equal to or greater than $\frac{1}{2}V_{DD}$, both paths 3 and 4 are activated and the output will be $\frac{1}{2}V_{DD}$. Moreover, when one or both of the inputs is around 0, both T3 and T4 are ON and the other paths to the output are disconnected, consequently the output is 0. In case of S = 2, T1 and T4 are OFF and the circuit implements the NAND functionality. During these operating conditions, the output will be determined based on paths 1 and 2. Finally, if S = 1 ($\frac{1}{2}V_{DD}$), all paths through the output will be disconnected and the output is HiZ. The principle operation of the proposed ternary OR/NOR is very similar to the AND/NAND circuit operation.

The proposed circuits utilize CNFETs with only two different diameters for their CNTs, while most of the designs of ternary logic gates in the literature need at least three distinct diameters. This property improves robustness to process variation and enhances the manufacturability of the proposed circuits.

3.3. Two-Digit Ternary Adder/Subtractor

Multi-digit ternary adder/subtractor has been designed using the proposed Buffer/Inverter. Figure 6 shows a two-digit adder/subtractor which can perform addition and subtraction by a selector signal S. when S=0, the outputs of the binary buffer and the ternary Buffer/Inverter are zero and A respectively, thus the circuit will add two digits. But, when S=2 (V_{DD}), the output of the binary buffer and the ternary Buffer/Inverter are 1 ($\frac{1}{2}V_{DD}$) and $\bar{A}$ respectively. Therefore, the circuit will perform

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subtraction. The applied binary buffer gets values 0 and 2 and produces 0 and 1 respectively. By using the proposed ternary Buffer/Inverter we would save *N* multiplexers for *N*-digit adder/subtractor circuit.

3.4. Ternary Arithmetic and Logic Unit (ALU)

In this section, we present two ternary arithmetic and logic units (ALUs). The proposed ALUs perform nine different logic and arithmetic operations. Table 3 shows the operations the ALUs. Figure 7 shows the first design which is based on multiplexers. The operations are controlled by two signals (S_0 and S_1) which are connected to the multiplexers selectors. When S_0 is 1, the ALU performs arithmetic operations (Addition, Subtraction and Increment), but when S_0 is 0 or 2, the ALU performs logic functions controlled by S_1 as shown in Table 3. This design is simple and modular but uses multiplexers which increases the transistor count, chip area, complexity and power consumption.

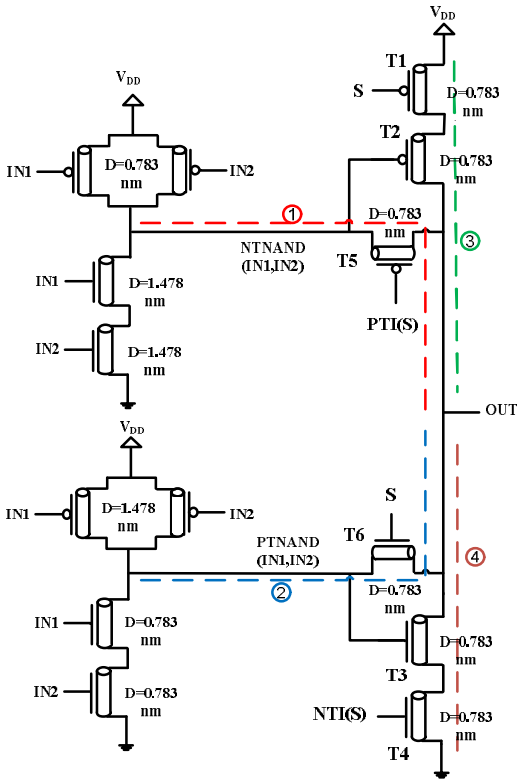

Figure 4. The circuit design of our proposed ternary AND/NAND. If S = 0, this circuit acts as an AND gate. If S = 2, it acts as a NAND gate, and if S = 1, the output is High Impedance (HZ).

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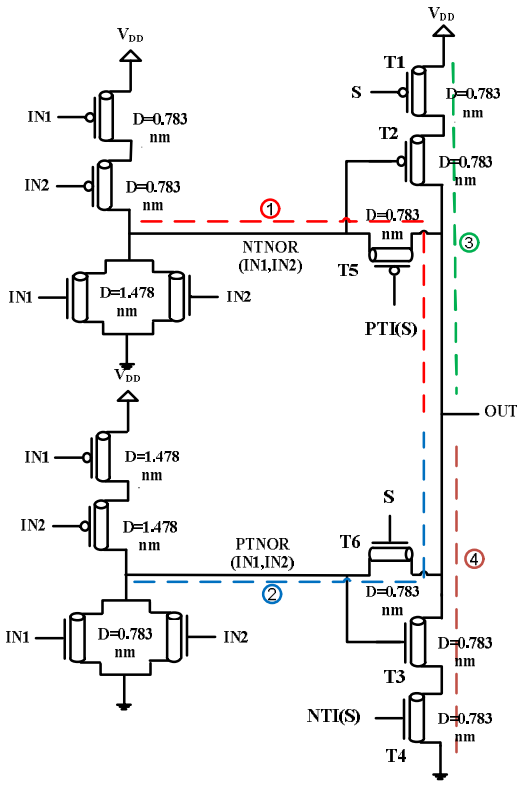

Figure 5. The circuit design of our proposed ternary OR/NOR gate. If S = 0, this circuit acts as an OR gate. If S = 2, it acts as a NOR gate, and if S = 1, the output is High Impedance (HZ).

To decrease the number of transistors and take advantage of the proposed ternary logic gates, we present the second ALU design which is shown in Fig. 8. In this design, we have eliminated the multiplexers by using the third state (HiZ) of the ternary gates proposed in Section III.

Four customized circuits have been designed to produce additional control signals (C_1, C_2, C_3 and C_4) for ternary gates by using two main control signals (S_0 and S_1). These circuits are shown in Fig. 9 and the output of each circuit is in Table 3.

Table 3 summarizes the functionality of the proposed ternary ALU. As it is indicated in Table 3, when S_0=1, the output of the logic unit is HiZ and the ALU performs an arithmetic operation based on the value of S_1. But, when S_0=0 or S_0=2, the output of the arithmetic unit will be HiZ by signal C_4, and by adjusting a proper value for the S_1 signal a desired logic function will be performed. For example, when S_0=0 and S_1=2, the C_3 output will be zero and C_1, C_2, and C_4 are 1.

Thus, the outputs of the two first logic gates (Buffer/Inverter and AND/NAND) and the arithmetic circuit are HiZ and consequently the ALU output will produce OR(A, B).

The proposed ALUs can have more functions by adding more control signals. Also, having HiZ state in the proposed ternary gates has two main advantages in the second design. (1) We do not need to use multiplexers in the ALU design which reduces area, complexity, and power consumption. (2) We can eliminate static power dissipation and improve power efficiency in unused traditional ternary gates.

Table 3. The truth table detailing the Operations and functionality of the presented ternary ALU and its control signals

S_0	S_1	C_1	C_2	C_3	C_4	Logic Unit Output	Arith Unit Output	ALU Output
1	0	1	1	1	0	HZ	Add	Add
1	1	1	1	1	0	HZ	Increase	Increase
1	2	1	1	1	0	HZ	Subtract	Subtract
0	0	0	1	1	1	Buffer	HZ	Buffer

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0	1	1	0	1	1	AND	HZ	AND
0	2	1	1	0	1	OR	HZ	OR
2	0	2	1	1	1	NOT	HZ	NOT
2	1	1	2	1	1	NAND	HZ	NAND
2	2	1	1	2	1	NOR	HZ	NOR

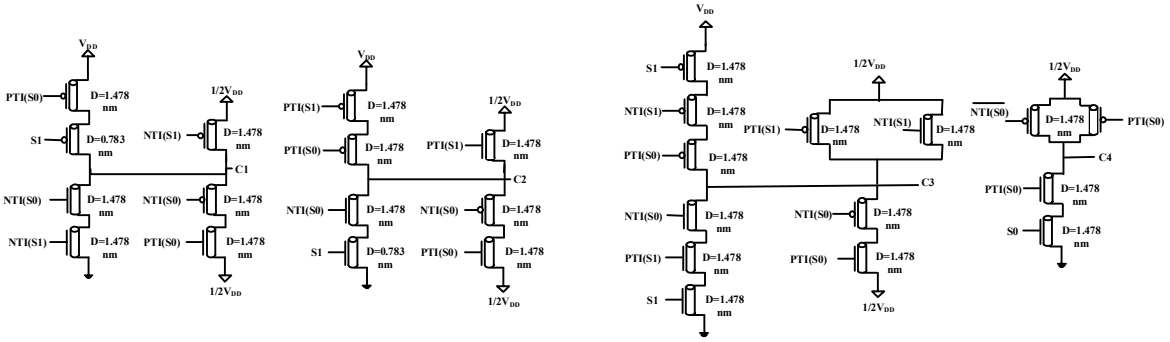

Figure 9. The Customized circuits to produce control signals using in the presented ALU. These circuits generate C1, C2, C3 and C4 signals which act as control signals for ternary basic gates in ALU.

4. Simulation Results

In this section, we present the simulation results of the proposed circuits. Simulations are conducted using the HSPICE simulator for 32 nm technology with the Stanford Compact SPICE model for CNFETs including the non-ideal and parasitic characteristics [33, 34]. Since this is the first attempt to design ternary logic gates with three output states, we could not compare our designs directly with state-of-the-art designs. Figure 10 shows the output waveforms of the presented circuits which confirms the correct operation of the designs.

Table 4 provides the simulation results of the ternary designs including delay, average power consumption and power delay product (PDP). As indicated in Table 4, the Buffer/NOT gate has the lowest delay. But due to the higher power consumption, it has a higher PDP compared to AND/NAND and OR/NOR designs. In order to have a fair comparison with previous ternary logic gates, we have simulated two-digit ternary adder/subtractor using the proposed designs and previous designs presented by Moaiyeri *et al.* [32], and the results are shown in Table 5. Based on the results using the proposed designs, a two-digit adder/subtractor could save power consumption more than 12X compared to Moaiyeri *et al.* [32]. Also, the PDP of the circuit using the proposed designs is about 5X better than the design of Moaiyeri *et al.* [32].

Moreover, we do sensitivity analysis for our proposed ternary circuits under different conditions and variations. We simulate the circuits with different temperatures from 0°C –

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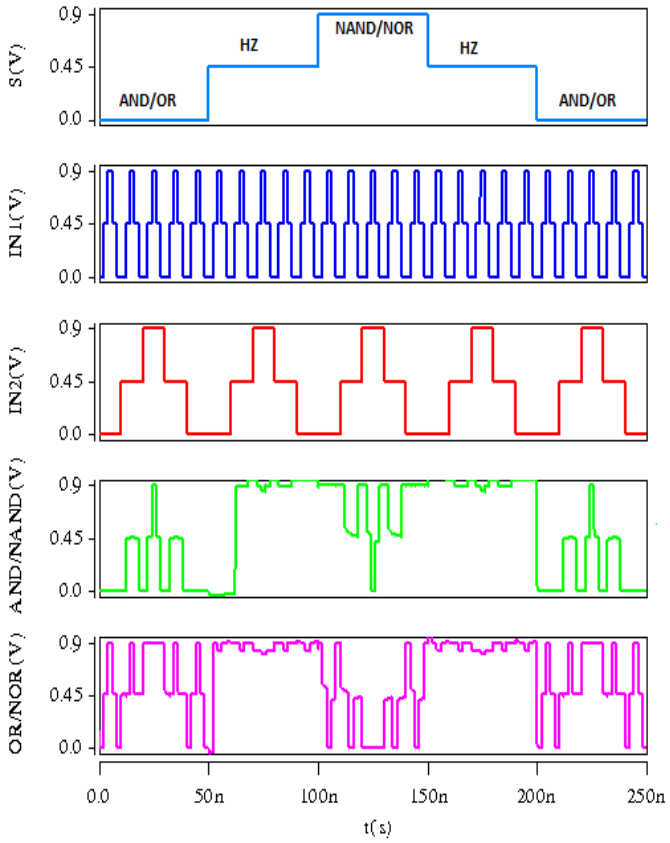

Figure 10. Output waveforms of the proposed ternary AND/NAND and OR/NOR gates. When S = 0, the circuits perform AND/OR functions. When S= 1, the output is high impedance. When S = 2, the circuits perform NAND/NOR operation.

Table 4. Delay, power and Power Delay Product (pdp) of our designed Circuits

Design	Delay (E-11s)	Maximum Delay (E-11s)	Power (E-7W)	PDP (E-17J)
Buffer	1.878	1.878	17.711	3.326
NOT	0.781			
AND	2.762	2.762	7.0485	1.946
NAND	1.202			
OR	2.732	2.732	10.54	2.879
NOR	1.314			

Table 5. Simulation results of two-digit ternary Add/Sub using the proposed designs and designs [11]

Design	**Maximum Delay (E-11s)**	**Power (E-7W)**	**PDP (E-17J)**
two Digit Add/Sub Using proposed designs	13.80	47.57	65.64
two Digit Add/Sub Using designs [32]	5.79	617.2	357.3

100°C. Figure 11 clearly shows that these designs have almost constant PDP for all temperatures due to the high thermal stability of CNFETs.

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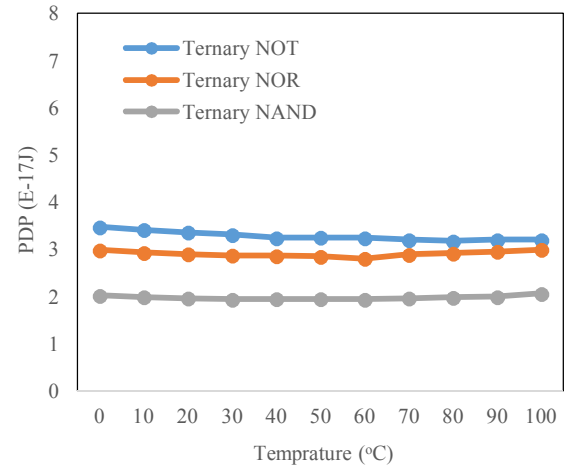

Figure 11. PDP variation against temperatures variation

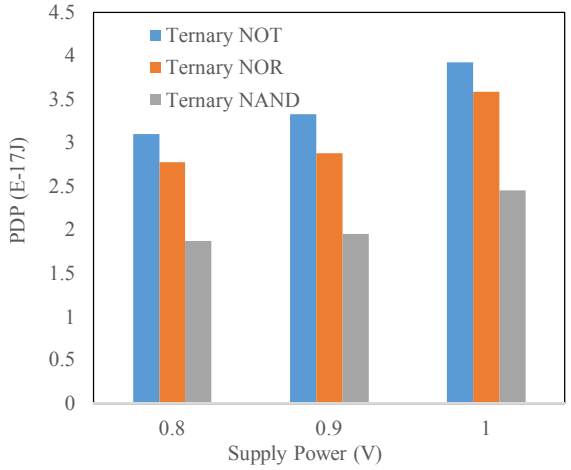

Figure 12. PDP variation in different supply voltages

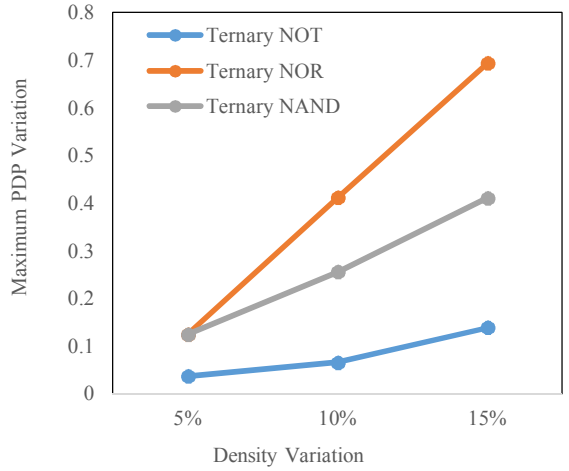

Figure 13. Maximum PDP variation against CNTs density variation. Density includes the CNT's pitch and the number of CNTs under gate.

Figure 12 shows the PDP variation of the circuits under different supply voltages. Designs are simulated in 0.8, 0.9 and 1V and the proposed ternary NAND gate has lower PDP because of its lower power consumption under all supply voltages.

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The operation of the ternary gates is also examined in the presence of process variation. One of the most important challenges in nanoscale devices is sensitivity to process variation, which can negatively impact the robustness of the circuits. It has been proven experimentally that the dominant source of variation in CNFET circuits is the nanotube density variations, which mainly results from variations in the spacing between CNTs on the substrate (*pitch*) and variations in the surviving CNT count after metallic CNT removal techniques [35]. Therefore, we used a Monte Carlo simulation to evaluate the CNT density variation with up to ±15% Gaussian distributions and variation at the ± 3σ levels. As in Fig. 13, all the designs show robustness against CNT density variation.

In Table 6, delay, power and PDP of the ternary ALUs have been presented. In this table logic and arithmetic units' delays are presented separately. As we have predicted, delay and power consumption of the first ALU are slightly more than the second ALU. The PDP of the first ALU is about 19% more than the second one.

Table 6. Delay, power and Power Delay Product (pdp) of ternary ALUs

Design	Logic Delay (E-11s)	Arith Delay (E-11s)	Power (E-6W)	PDP (E-17J)
1st ALU	2.175	6.699	13.11	87.82
2nd ALU	1.652	6.307	11.68	73.66

5. Conclusion

In this paper, we present three output-states ternary logic circuits. Each of the presented circuits can perform a logic function or its complement via a control signal. When the circuits are idle *i.e.* not in use, the output is high impedance (HiZ), which lowers the power consumption. We design these circuits using carbon nano-tube field effect transistors (CNFETs). CNFETs are very appropriate for designing MVL circuits because of their ability to set the desired threshold voltage by adjusting the tubes' diameters. Moreover, two-digit adder/subtractor and two ternary ALUs have been designed using the proposed gates. The second ALU can reach the power efficiency by using the high impedance (HiZ) state of the gates when they are not in use. Circuits are simulated using HSPICE simulator with 32nm CNFET technology under different conditions. The results show robustness under process variation, temperature, and supply voltage. The AND/NAND gate has the lowest PDP compared to the other proposed designs because of its lower power dissipation. It has almost 48% lower PDP compared to the OR/NOR gate. Also by using the proposed designs in two-digit adder/subtractor, the power consumption is reduced more than 12X compared to the state-of-the-are designs.

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References

1. A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," *IEEE Transactions on Nanotechnology*, vol. 4, pp. 168-179, 200
2. E. Dubrova, "Multiple-valued logic in vlsi: Challenges and opportunities," in *Proceedings of NORCHIP*, 1999, pp. 340-350.
3. S. L. Hurst, "Multiple-valued logic—Its status and its future," *IEEE Transactions on Computers*, vol. 12, pp. 1160-1179, 1984.
4. S. Tabrizchi, A. Panahi, F. Sharifi, K. Navi, and N. Bagherzadeh, "A novel method for designing ternary adder cell based on CNFETs," *IET Circuits, Devices & Systems*, 2017.
5. S. Lin, Y.-B. Kim, and F. Lombardi, "Design of a CNTFET-based SRAM cell by dual-chirality selection," *IEEE Transactions on Nanotechnology*, vol. 9, pp. 30-37, 2010.
6. K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, pp. 305-327, 2003.

7. F. Sharifi, A. Panahi, H. Sharifi, K. Navi, N. Bagherzadeh, and H. Thapliyal, "Design of quaternary 4–2 and 5–2 compressors for nanotechnology," *Computers & Electrical Engineering*, vol. 56, pp. 64-74, 2016.
8. W. Porod, C. Lent, G. H. Bernstein, A. O. Orlov, I. Hamlani, G. L. Snider, *et al.*, "Quantum-dot cellular automata: computing with coupled quantum dots," *International Journal of Electronics*, vol. 86, pp. 549-590, 1999.
9. G. Deng and C. Chen, "Binary multiplication using hybrid MOS and multi-gate single-electron transistors," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 21, pp. 1573-1582, 2013.
10. Y.-B. Kim, "Challenges for nanoscale MOSFETs and emerging nanoelectronics," *Transactions on Electrical and Electronic Materials*, vol. 11, pp. 93-105, 2010.
11. M. H. Moaiyeri, K. Navi, and O. Hashemipour, "Design and evaluation of CNFET-based quaternary circuits," *Circuits, Systems, and Signal Processing*, vol. 31, pp. 1631-1652, 2012.
12. S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE transactions on nanotechnology*, vol. 10, pp. 217-225, 2011.
13. H. Mouftah and I. Jordan, "Implementation of 3-valued logic with cosmos integrated circuits," *Electronics Letters*, vol. 10, pp. 441-442, 1974.
14. H. Mouftah and K. Smith, "Injected voltage low-power CMOS for 3-valued logic," in *IEE Proceedings G-Electronic Circuits and Systems*, 1982, pp. 270-272.
15. R. C. G. da Silva, H. Boudinov, and L. Carro, "A novel voltage-mode CMOS quaternary logic design," *IEEE Transactions on Electron devices*, vol. 53, pp. 1480-1483, 2006.
16. S. R. R. Datla and M. A. Thornton, "Quaternary voltage-mode logic cells and fixed-point multiplication circuits," in *Multiple-Valued Logic (ISMVL), 2010 40th IEEE International Symposium on*, 2010, pp. 128-133.
17. A. Heung and H. Mouftah, "Depletion/enhancement CMOS for a lower power family of three-valued logic circuits," *IEEE Journal of Solid-State Circuits*, vol. 20, pp. 609-616, 1985.
18. I. Thoidis, D. Soudris, I. Karafyllidis, S. Christoforidis, and A. Thanailakis, "Quaternary voltage-mode CMOS circuits for multiple-valued logic," *IEE Proceedings-Circuits, Devices and Systems*, vol. 145, pp. 71-77, 1998.
19. V. P. KS and K. Gurumurthy, "Quaternary CMOS combinational logic circuits," in *Information and Multimedia Technology, 2009. ICIMT'09. International Conference on*, 2009, pp. 538-542.
20. Y. Yasuda, Y. Tokuda, S. Zaima, K. Pak, T. Nakamura, and A. Yoshida, "Realization of quaternary logic circuits by n-channel MOS devices," *IEEE Journal of Solid-State Circuits*, vol. 21, pp. 162-168, 1986.
21. J. Liang, L. Chen, J. Han, and F. Lombardi, "Design and evaluation of multiple valued logic gates using pseudo N-type carbon nanotube FETs," *IEEE Transactions on Nanotechnology*, vol. 13, pp. 695-708, 2014.
22. S. Tabrizchi, F. Sharifi, Z. M. Saifulla, and A. H. Badawy, "Enabling Energy-Efficient Ternary Logic Gates using CNFETs," in *17th IEEE International Conference on Nanotechnology*, 2017,
23. I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent, and G. L. Snider, "Digital logic gate using quantum-dot cellular automata," *science*, vol. 284, pp. 289-291, 1999.
24. V. V. Zhirnov, J. A. Hutchby, G. Bourianoffls, and J. E. Brewer, "Emerging research logic devices," *IEEE Circuits and Devices Magazine*, vol. 21, pp. 37-46, 2005.
25. J. Deng, "Device modeling and circuit performance evaluation for nanoscale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors," Stanford University, 2007.
26. Y. B. Kim, Y.-B. Kim, and F. Lombardi, "A novel design methodology to optimize the speed and power of the CNTFET circuits," in *Circuits and Systems, 2009. MWSCAS'09. 52nd IEEE International Midwest Symposium on*, 2009, pp. 1130-1133.
27. B. Wang, C.P. Poa, L. Wei, L.J. Li, Y. Yang and y. Chen, "(n, m) selectivity of single-walled carbon nanotubes by different carbon precursors on Co-Mo catalysts" *Journal of the American Chemical Society*, vol. 129, pp. 9014-9019.
28. A. Lin , N. Patil, K. Roy, A. Badmaev, L.G. De Arco, C. Zhou, S. Mitra and H.-S.P. Wong, "Threshold voltage and on–off ratio tuning for multiple-tube carbon nanotube FETs,", *Nanotechnology, IEEE Transactions on*, vol. 8, pp. 4-9, 2009.
29. H. Park, A. Afzali, S.-J. Han, G. S. Tulevski, A. D. Franklin, J. Tersoff, *et al.*, "High-density integration of carbon nanotubes via chemical self-assembly," *Nature nanotechnology*, vol. 7, pp. 787-791, 2012.
30. N. Patil, J. Deng, H.-S. Wong, and S. Mitra, "Automated design of misaligned-carbon-nanotube-immune circuits," in *Proceedings of the 44th annual Design Automation Conference*, 2007, pp. 958-961.

31. S. C. Kleene, N. de Bruijn, J. de Groot, and A. C. Zaanen, *Introduction to metamathematics* vol. 483: van Nostrand New York, 1952.
32. M. H. Moaiyeri, A. Doostaregan, and K. Navi, "Design of energy-efficient and robust ternary circuits for nanotechnology," *IET Circuits, Devices & Systems,* vol. 5, pp. 285-296, 2011.
33. J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking," *IEEE Transactions on Electron Devices,* vol. 54, pp. 3195-3205, 2007.
34. J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region," *IEEE Transactions on Electron Devices,* vol. 54, pp. 3186-3194, 2007.
35. J. Zhang, N. Patil, H.-S. P. Wong, and S. Mitra, "Overcoming carbon nanotube variations through co-optimized technology and circuit design," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 4.6. 1-4.6. 4.