Article

A Thermally Stable Quasi-CMOS Bipolar Logic

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Abstract: Logic gates made of pairs of NPN and PNP bipolar transistors, similar to CMOS logic gates, have been proposed and patented long ago but did not find any practical application until now. Other bipolar technologies (TTL, TTL-S, ECL), once the technologies of choice for digital systems, were abandoned and superseded by CMOS. In this paper it is shown that now, when truly complementary pairs of bipolar transistors can be made, properly biased bipolar gates similar to CMOS gates are feasible, can be thermally stable and find practical applications.

Keywords: bipolar logic; bipolar transistor; thermal stability; bipolar inverter; PD-SOI, FD-SOI

!. Introduction

Bipolar technologies such as TTL, TTL-S, ECL, once the technologies of choice for digital systems, were totally abandoned and superseded by CMOS. The reasons are well known: large area of vertical bipolar transistors in comparison with MOS devices, larger device count in bipolar logic gates and larger power consumption. These properties made bipolar technologies mentioned above unsuitable for VLSI circuits. CMOS-like complementary bipolar logic gates similar to CMOS logic gates (Figure 1) have been proposed long ago (1976, [1]) but never used. They will be called CBIP in this paper. In traditional bipolar technologies, in which TTL or ECL gates were made, good NPN vertical bipolar transistors were available but PNP transistors had different physical structures and much worse parameters. They were not complementary to their NPN counterparts. Moreover, vertical transistors were strongly asymmetric, with heavily doped emitter, much lower doping in the collector and different areas of emitter-base and collector-base junctions. Such transistors have relatively high voltage drop between emitter and collector when switched "on" in a digital gate. As a result, both "0" and "1" voltage levels would be degraded ("0" voltage level higher than 0 and "1" voltage level lower than supply voltage) if asymmetric transistors were used in a CMOS-like digital gate.
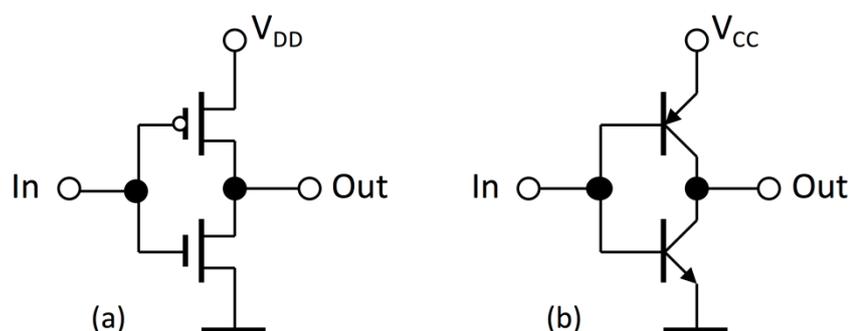

Figure 1. Simplest logic gates: (a) inverter CMOS, (b) bipolar inverter CBIP.

In 2011 a new structure of a lateral bipolar transistor on SOI, technologically compatible with PD-SOI (Partially Depleted Silicon on Insulator) CMOS circuits, has been

demonstrated [2]. Such transistors are small and symmetric, complementary pairs of NPN and PNP devices can be made. Later in a series of papers [3-7] these transistors were investigated both theoretically and experimentally, including experimental characterization of inverters, SRAM cell flip-flops and ring oscillators. It was suggested that CMOS-like bipolar logic, i.e. logic gates made of complementary pairs of NPN and PNP transistors, could be useful both for very fast circuits and very low power circuits. Later another SOI-based technology, in which complementary pairs of symmetric NPN and PNP transistors as well as MOS devices can be made, has been demonstrated [9,10]. One more bipolar device concept – symmetric lateral doping-free bipolar transistor – has been proposed [11] and investigated [12,13]. In spite of these very promising works CMOS-like bipolar logic is still not used in digital integrated circuits.

There is a fundamental difference between CMOS logic gates and similar CBIP logic gates: the input current. In MOS transistors the input (gate) current is equal to zero (except gate leakage that is negligible in state-of-the-art very small devices) while in bipolar transistors the input (base) current in the "on" state is not negligible. When the output of a CBIP gate is connected to the input of another CBIP gate, the current drawn by this input from the output of the previous gate (as shown in Figure 2) distorts the voltage transfer curve of the previous gate.
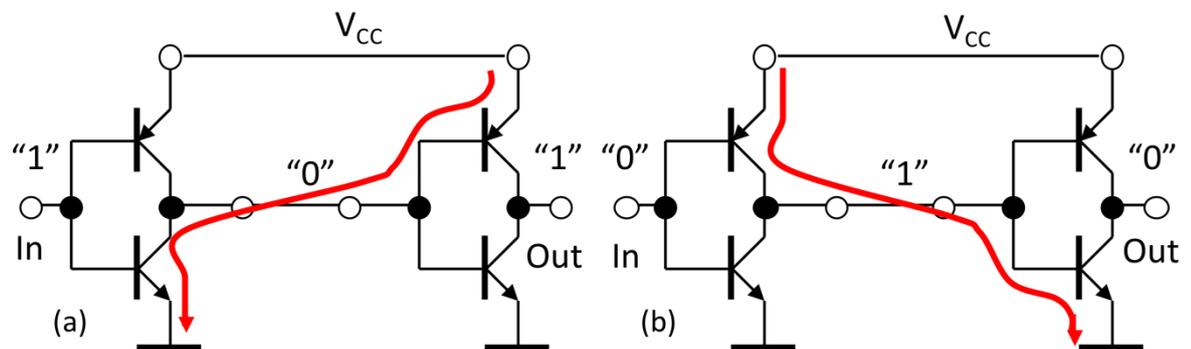

Figure 2. Currents in a pair of CBIP inverters: (a) with "1" at input, (b) with "0" at input

The input (base) currents in CBIP gates depend exponentially on the input (base-emitter) voltages and rise exponentially with temperature. This thermal effect is highly undesirable and makes CBIP-based logic circuits practically useless at elevated temperatures. In this paper a simple solution mitigating this effect is proposed in Section 2. In Section 3 the properties of CBIP gates performing NOT, NOR and NAND logic functions are discussed in the context of the solution of the thermal problem proposed in Section 2. Examples of CBIP-based logic circuits are also shown. Section 4 discusses the results shown in previous Sections and suggests possible applications of CBIP circuits. Transistor models used in simulations are given in Appendix. These models roughly correspond to the experimental characteristics of NPN devices discussed in [2, Fig.9]. To simplify interpretation of the simulation results, in most cases it is assumed that the models of NPN and PNP devices are identical.

2. Thermal stability of CBIP gates

Let us consider a CBIP inverter biased as in Figure 3. It is assumed that the voltage level of logic "1" equals the supply voltage V_{CC}.
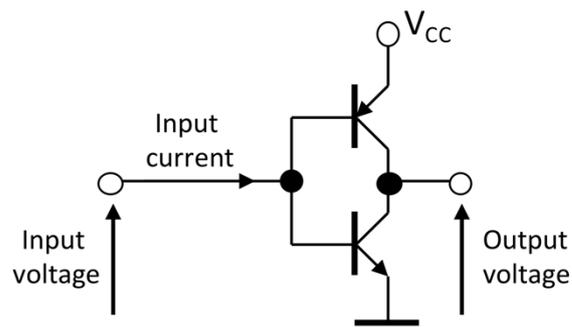
Figure 3. Simulated CBIP inverter

Figure 4 shows simulated DC transfer characteristic and input current vs. input voltage for V_{CC}=1V at 300K. The transfer characteristic is excellent, but the input current is unacceptable – up to 0,7 mA.
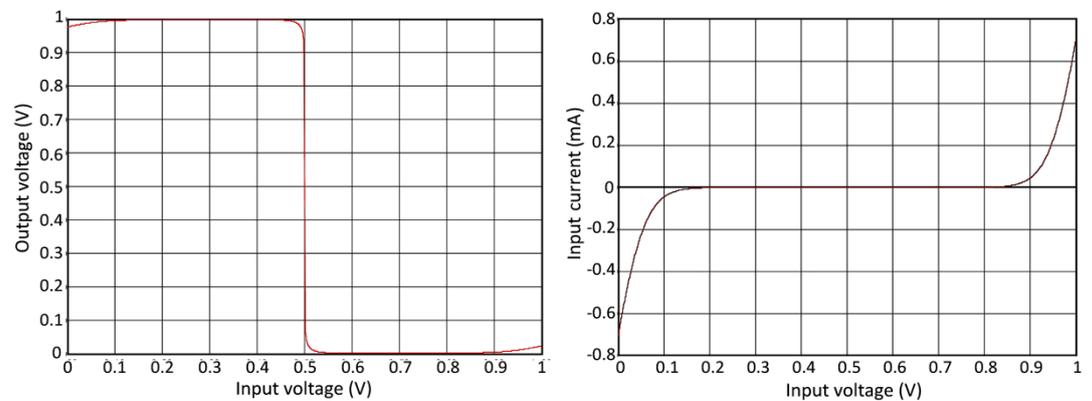

Figure 4. Transfer characteristic and input current of a CBIP inverter. V_{CC}=1V, temperature 300K.

If the supply voltage is reduced to 0.65 V, the transfer characteristic is still acceptable, and the input current is reduced to nanoamperes – see Figure 5.
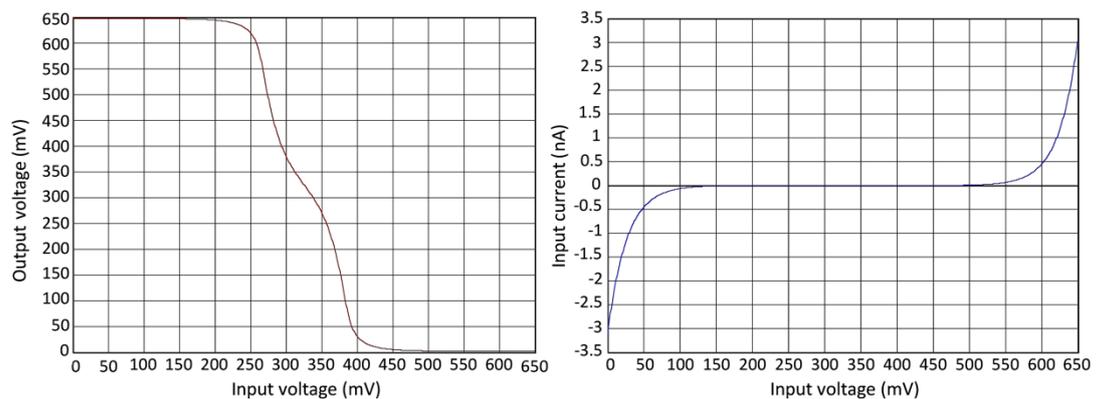

Figure 5. Transfer characteristic and input current of a CBIP inverter. V_{CC}=0.65V, temperature 300K.

However, reduction of the supply voltage does not solve the problem of the input current because this current strongly increases with temperature. Figure 6 shows the

transfer characteristic and input current at 400K. The input current increases from 3 nA to 600 nA.
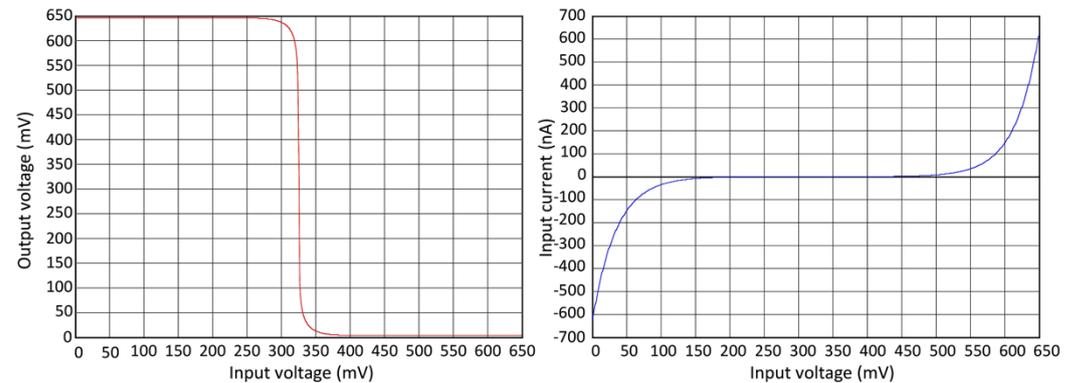

Figure 6. Transfer characteristic and input current of a CBIP inverter. V_{CC}=0.65V, temperature 400K.

To mitigate this thermal effect, a solution borrowed from analog domain can be used. Figure 7 shows this solution. The supply voltage for the CBIP inverter Q2-Q3 equals the base-emitter voltage of transistor Q1. This voltage also defines the logic level "1". With "1" (i.e. V_{supply}) at the input of the inverter transistors Q1 and Q2 make the current mirror. If both are identical and their temperatures are identical, both collector currents are the same (neglecting base currents). If the collector current of Q1 (determined by the V_{CC} voltage and resistance R) does not depend on temperature, the collector current of Q2 also does not depend on temperature. The input current of the inverter will be h$_{FE}$ – times lower. It will depend somewhat on temperature because h$_{FE}$ is temperature-dependent, but this dependence is rather weak, not exponential.

It is worth noting that Q1 and Q2 need not be identical. If they aren't, the collector current of Q2 will be proportional to the collector current of Q1. If the collector current of Q1 does not depend on temperature, the collector current of Q2 will not depend as well.
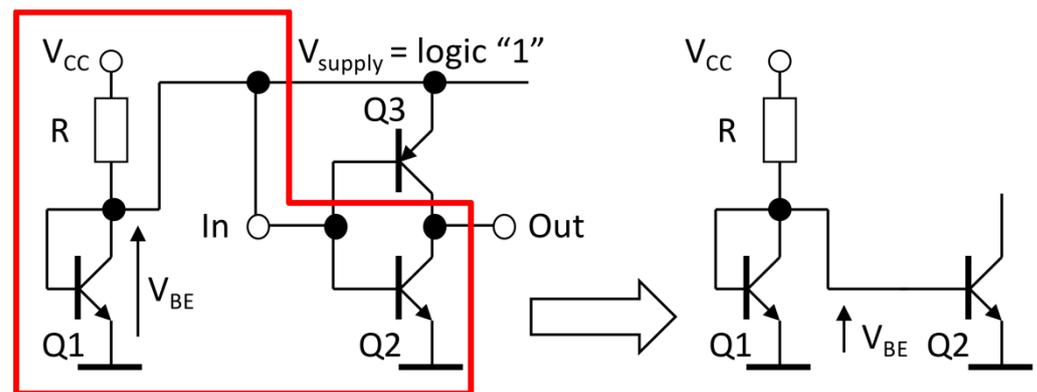

Figure 7. The concept of thermal stabilization of CBIP gates: with "1" at the input of the inverter Q1 and Q2 make the current mirror.

If the logic level at the input of the inverter is "0", current mirror is composed of transistors Q1 and Q3 – see Figure 8. The base-emitter voltages of Q1 and Q3 are identical. In the general case Q1 (an NPN device) and Q3 (a PNP device) will not be identical but since the collector current of Q1 is temperature-independent, thermal stability of the inverter will be maintained. To demonstrate this, simulations shown in Figure 9 and Figure 10 were carried out with NPN model different from PNP model – see Appendix. The input current characteristics are no longer symmetric but the input current at 400K is almost the same as at 300K.
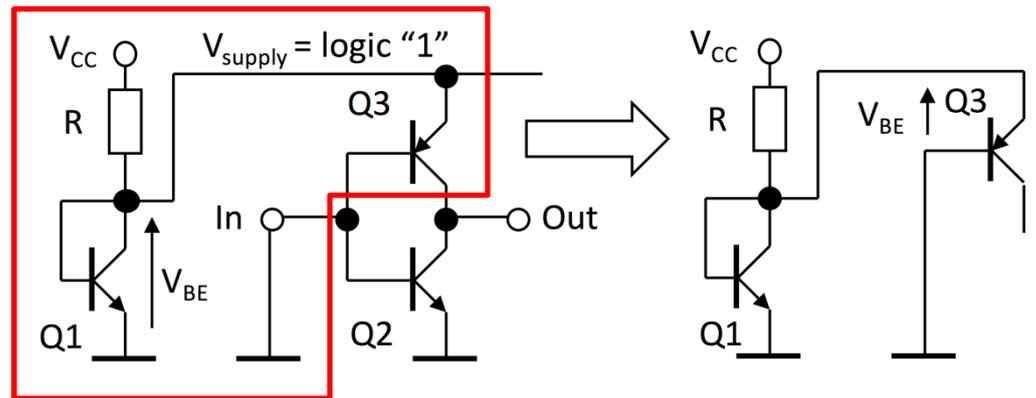
Figure 8. The concept of thermal stabilization of CBIP gates: with "0" at the input of the inverter Q1 and Q3 make the current mirror.
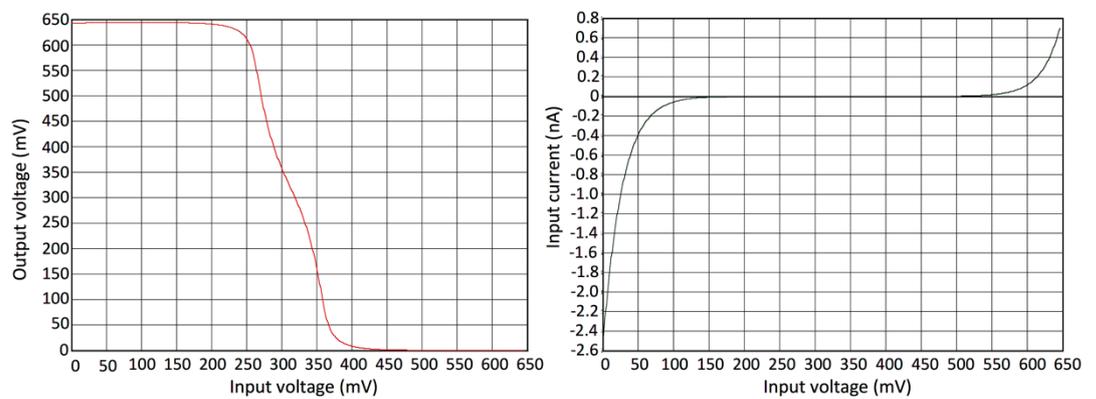

Figure 9. Transfer characteristic and input current of a thermally stabilized CBIP inverter (Figures 7 and 8). V_{CC} = 1V, R=10MW, temperature 300K.

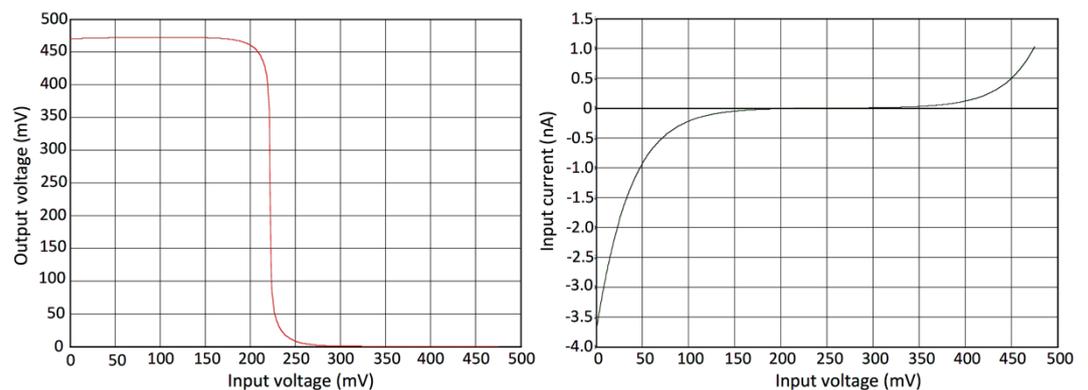

Figure 10. Transfer characteristic and input current of a thermally stabilized CBIP inverter (Figures 7 and 8). V_{CC} = 1V, R=10MΩ, temperature 400K.

The thermal stabilization idea shown in Figures 7 and 8 can be extended to logic blocks with any number of CBIP inverters and other gates, as shown in Figure 11. By varying R one can vary the sum of all currents consumed by the logic gates in this block, i.e. the overall current consumption. Of course, thermal stabilization of the whole block requires the same temperature of Q1 and all the transistors in the logic block.
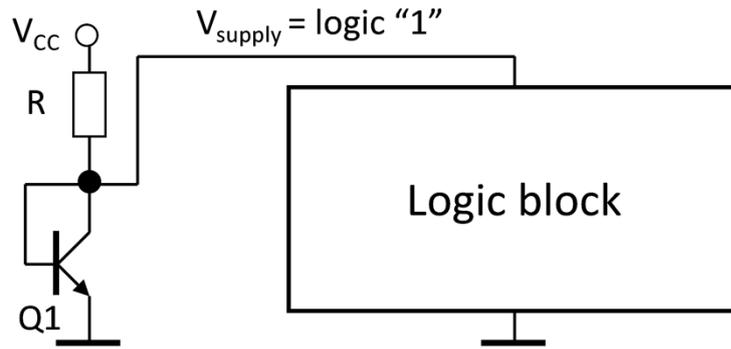
Figure 11. Thermally stabilized logic block.

Note that increase of the temperature from 300K to 400K results in reduction of the supply voltage, which is also the "1" voltage level, from 650 mV to 465 mV (Figures 9 and 10). This is not a problem in a digital circuit if the supply voltage and the "1" voltage level are the same for all CBIP gates in the circuit, as in Figure 11. Examples are shown in the next Section.

3. CBIP gates and circuits

3.1 NAND and NOR gates

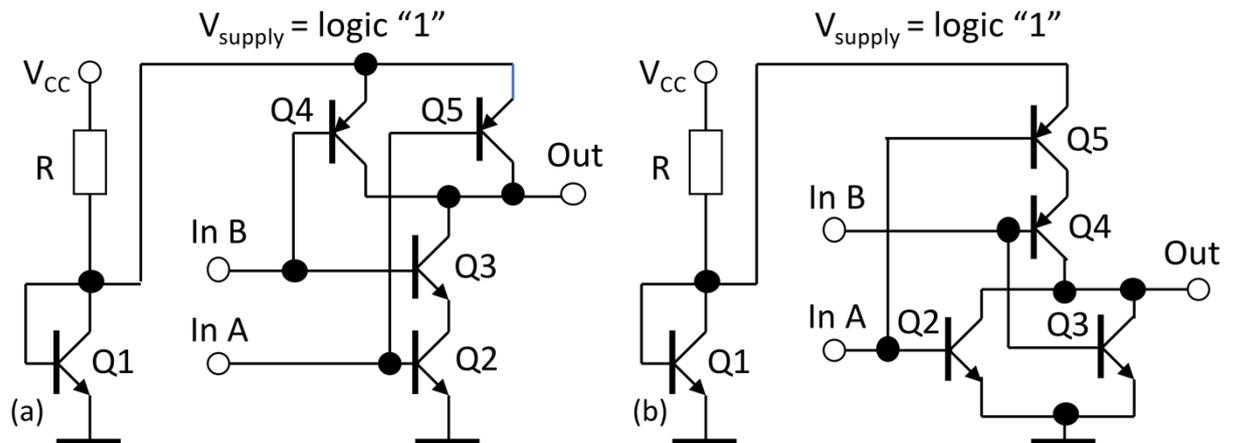The schematic diagrams of NAND and NOR gates are shown in Figure 12.

Figure 12. Thermally stabilized CBIP gates. (a) NAND gate, (b) NOR gate.

Figure 13 shows the transfer characteristics of the NAND and NOR gates. Characteristics (b) and (c) are similar to characteristics of CMOS gates. Characteristics (a) are different, somewhat similar to transfer characteristics of logic gates in the old NMOS technology with NMOS enhancement mode transistors as active devices and NMOS depletion mode transistor as pull-up device. Although the (a) characteristics are not as good as (b) and (c) characteristics, the NAND and NOR gates work correctly in logic circuits, as it will be demonstrated in subsection 3.4.
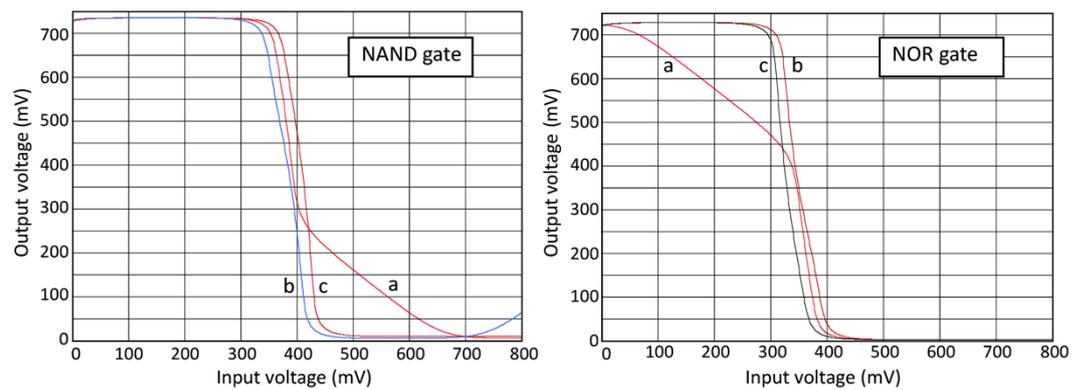
Figure 13. Transfer characteristics of NAND and NOR gates. V_{CC}=1V, R=500kΩ, temperature 300K. NAND: (a) IN A: 0…800 mV, IN B: 700 mV; (b) IN A: 700 mV, IN B: 0…800 mV; (c) IN A=IN B: 0…800 mV. NOR: (a) IN A: 0…800 mV, IN B: 0; (b) IN A: 0, IN B: 0…800 mV; (c) IN A=IN B: 0…800 mV.

3.2 AND and OR gates

By adding inverters at outputs of NAND and NOR gates we obtain AND and OR gates (Figure 14).
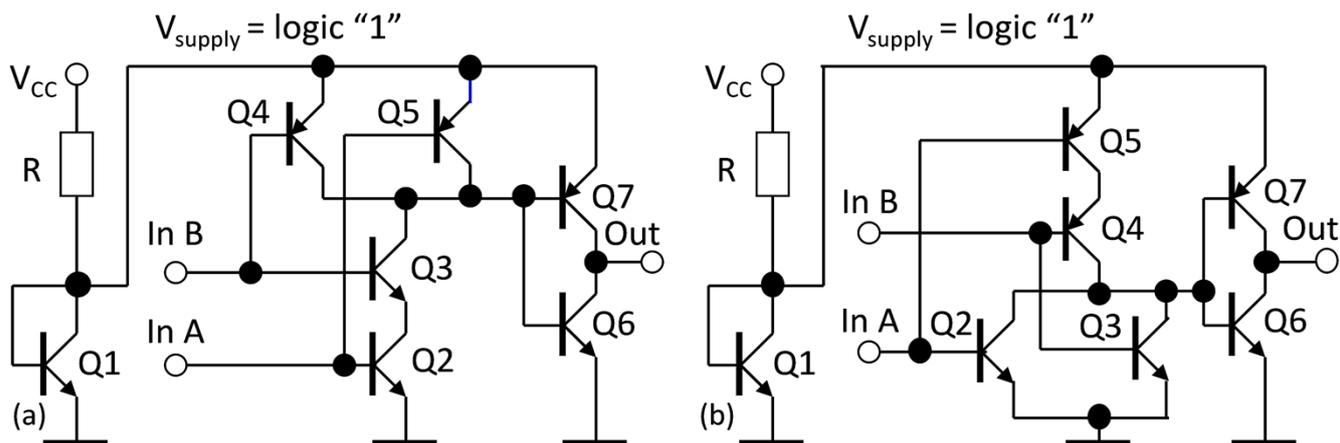

Figure 14. Thermally stabilized CBIP gates. (a) AND gate, (b) OR gate.

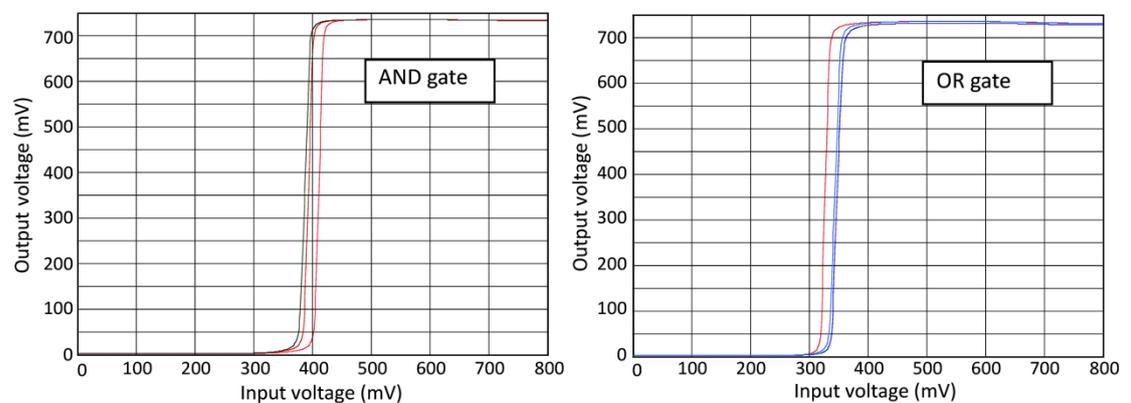Figure 15 shows transfer characteristics of these gates.

Figure 15. Transfer characteristics of AND and OR gates. VCC=1V, R=500kW, temperature 300K. AND: All three characteristics are almost the same. OR: All three characteristics are almost the same.

3.3. The effects of load

All transfer characteristics shown above (Figures 4,5,6,9,10,13 and 15) were obtained for gates without any load connected to their outputs. Figure 16 shows inverters with resistive load (a) and load in the form of input of another inverter (b).
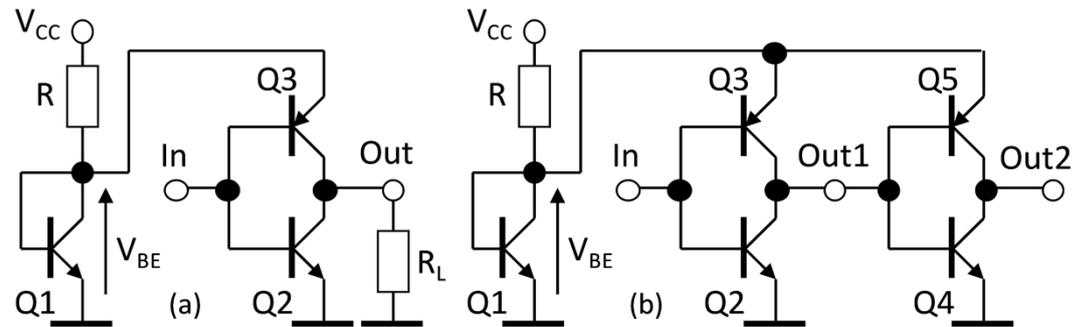

Figure 16. Inverters with resistive load (a) and nonlinear load – input of another inverter (b).

The maximum current that can be drawn from output of any gate will never exceed the current supplied from V_{CC}: $I_{max} = (V_{CC} - V_{BE})/R$. In practice this means that the load resistance R_L must be much larger than R. However, even resistive load that meets this requirement will shift the transfer characteristics of the gate. This is shown in Figure 17a.
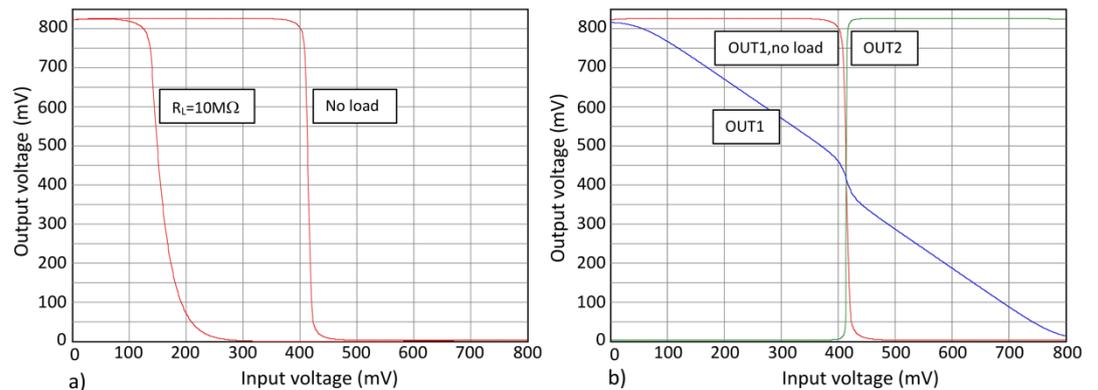
Figure 17. Transfer characteristics of inverter with resistive load (a) and inverter with nonlinear load (input of another inverter - b). V_{CC}=1V, R=10kΩ, temperature 300K.

If the output of a CBIP gate is connected to the input of another CBIP gate, as in Figure 16b, the transfer characteristic of the first gate is strongly distorted, as shown in Figure 17b. However, the transfer characteristic from the input to the output of the second gate is correct. In the next subsection it is demonstrated that logic blocks with CBIP gates work correctly despite distortion shown in Figure 17b.

3.4. Two examples

The first example demonstrates operation of a simple logic block (C17 ISCAS benchmark) implemented with CBIP gates. The logic diagram of C17 benchmark is shown in Figure 18. The block is thermally stabilized in the way shown in Figure 11.
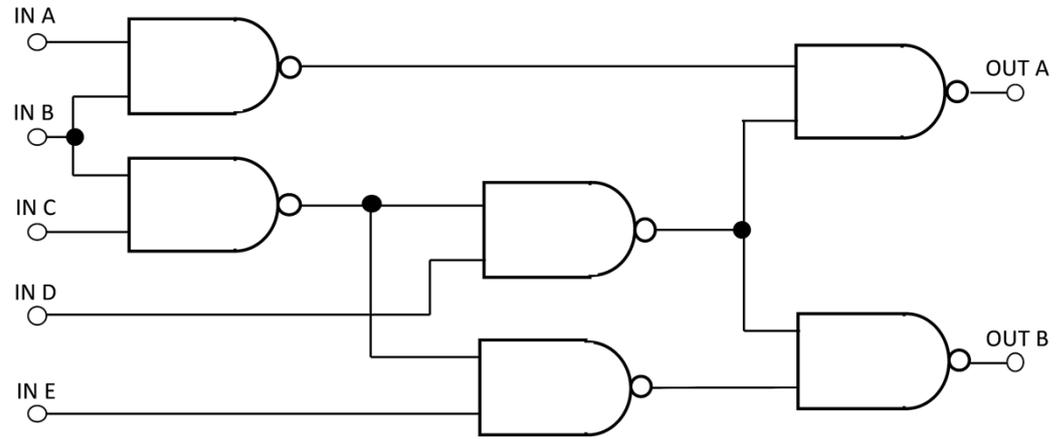
Figure 18. The logic diagram of the C17 ISCAS benchmark.

The input and output signals are shown in Figure 19. For comparison operation of the same block implemented with 22nm CMOS gates is shown. The logical response of the CBIP-based block does not differ from response of CMOS-based block.
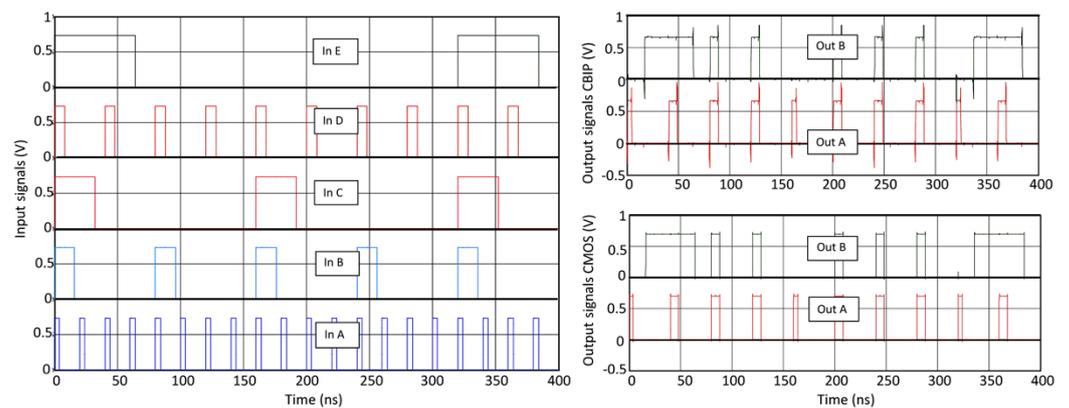
Figure 19. Operation of the ISCAS C17 benchmark: CBIP and 22 nm CMOS implementation. CBIP: V_{CC}=1V, R=3MΩ. CMOS: V_{DD}=0.7V. Temperature 300K in both cases.

It has been demonstrated [4,6] that delay of a CBIP inverter can vary by many orders of magnitude by varying its supply voltage. The performance of CBIP-based thermally stabilized digital circuits can be adjusted by the voltage V_{CC} and/or resistance R. The second example demonstrates this feature by replacing resistor R by a NMOS transistor, whose gate voltage is controlled by a voltage source V_{REG} (Figure 20). By varying this voltage the supply voltage and the frequency of oscillation of the ring oscillator are varied.

Figure 20. Five stage CBIP ring oscillator with supply voltage controlled by a NMOS transistor.

Figure 21. Operation of five stage CBIP ring oscillator with supply voltage controlled by a NMOS transistor: control voltage, supply current (log scale) and output voltage as a function of time; V_{CC}=1.2V, temperature 300K.

Figure 21 shows how the CBIP ring oscillator can be used as a voltage-controlled oscillator. The shortest oscillation period at V_{REG}=1.5V equals 0.28 ns, the longest period at V_{REG}=0.95V is approximately 125 ns. This simulation de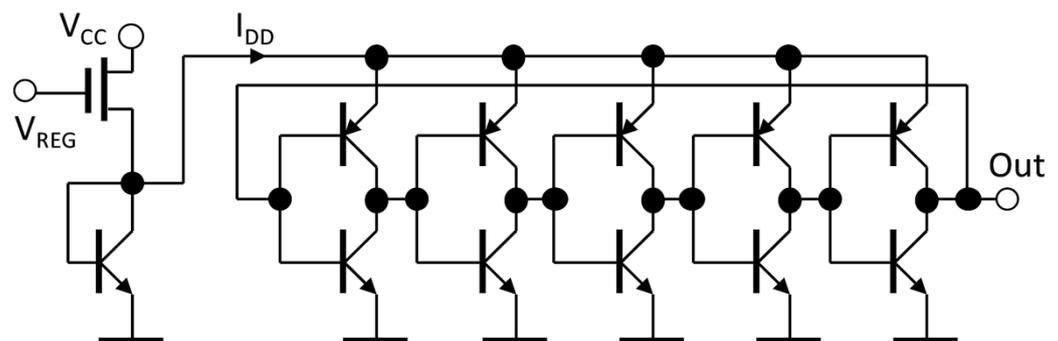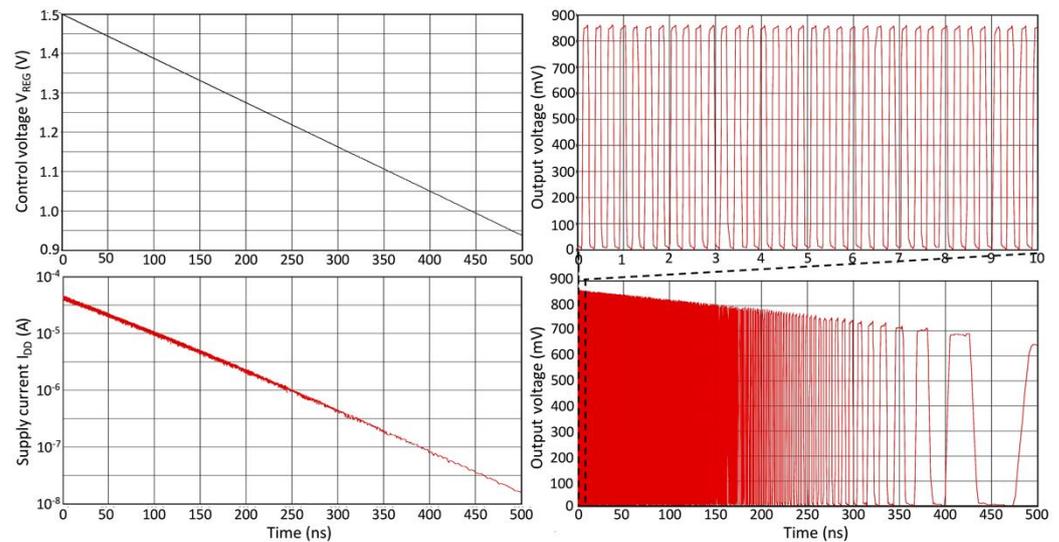monstrates flexibility of CBIP-based logic circuits: the same circuit can be used either as a high performance circuit or as a low power circuit by changing the V_{CC} voltage and/or the resistance R (Figures 7 and 8). If the resistance R is replaced by an active voltage-controlled device, as in Figure 20, the performance and power consumption can be easily controlled in a working circuit and adjusted as needed for a given task.

4. Discussion and conclusions

The results of the simulations show that CBIP gates thermally stabilized as shown in Figures 7 and 8 can be used to build fully functional digital circuits working well in a broad range of temperatures. A unique feature of CBIP-based digital circuits is that the same circuit can be used either as a ultra-low power circuit or as a high performance circuit, and power vs. performance tradeoff can be easily controlled in a working circuit.

But the question is: who needs CBIP gates?

It is rather obvious that CBIP-based digital circuits will not replace the most advanced FinFet or Nanosheet-based CMOS circuits. However, they can be technologically compatible with more traditional CMOS circuits. The symmetric lateral bipolar transistors on PD-SOI substrates [2-7] and CBIP gates using them could be used as additional components of PD-SOI CMOS circuits, for example in I/O buffers, or even as either high performance or ultra-low power digital blocks. The doping-free symmetric lateral bipolar transistors [11-13] could become a valuable addition to FD-SOI (Fully Depleted Silicon on Insulator) CMOS circuits, where channel area of MOS devices is not intentionally doped.

It is worth noting that bipolar transistors are very useful in analog circuits. In mixed-signal circuits the symmetric lateral bipolar transistors could be used e.g. in low noise amplifiers as well as in RF amplifiers. This topic is, however, beyond the scope of this paper.

Conflicts of Interest: The author declares no conflict of interest.

Appendix

Below are listed device models in Berkeley Spice format used in the simulations reported above.

Bipolar transistor models identical for NPN and PNP devices:
.MODEL QMODN NPN(is=2e-19 bf=10 br=10 re=20 rb=20 var=25 vaf=25 ikf=5.15e-4
+ikr = 5.15e-4 cje=6e-17 cjc=6e-17 vjc=1 vje=1 tf=4.2e-12 tr=4.2e-12)
.MODEL QMODP PNP(is=2e-19 bf=10 br=10 re=20 rb=20 var=25 vaf=25 ikf=5.15e-4
+ikr = 5.15e-4 cje=6e-17 cjc=6e-17 vjc=1 vje=1 tf=4.2e-12 tr=4.2e-12)

Bipolar transistor models – NPN device with higher h_{FE} than PNP device, used in simulations shown in Figures 9, 10, 19 and 21:
.MODEL QMODN NPN(is=5e-19 bf=100 br=100 re=20 rb=20 var=25 vaf=25 ikf=5.15e-4
+ikr = 5.15e-4 cje=2e-18 cjc=2e-18 vjc=1 vje=1 tf=4.2e-12 tr=4.2e-12)
.MODEL QMODP PNP(is=2e-19 bf=10 br=10 re=20 rb=20 var=25 vaf=25 ikf=5.15e-4
+ikr = 5.15e-4 cje=2e-18 cjc=2e-18 vjc=1 vje=1 tf=4.2e-12 tr=4.2e-12)

Generic NMOS model for 22 nm CMOS technology [14], used in simulations shown in Figure 21:
* PTM High Performance 22nm Metal Gate / High-K / Strained-Si
.model   nmos   nmos   level = 14

+version = 4.6.5 binunit = 1 paramchk= 1 mobmod   = 0
+capmod   = 2 igcmod   = 1 igbmod   = 1 geomod   = 1
+diomod   = 1 rdsmod   = 0 rbodymod= 1 rgatemod= 1
+permod   = 1 acnqsmod= 0 trnqsmod= 0
+tnom   = 27 toxe   = 1.05e-009 toxp   = 8e-010 toxm = 1.05e-009
+dtox = 2.5e-010 epsrox   = 3.9 wint = 5e-009 lint = 2e-009
+ll = 0 wl = 0 lln = 1 wln = 1
+lw = 0   ww = 0 lwn = 1 wwn = 1
+lwl = 0   wwl = 0 xpart   = 0 toxref   = 1.05e-009
+xl   = -9e-9

+vth0 = 0.50308   k1   = 0.4   k2   = 0 k3   = 0
+k3b   = 0 w0   = 2.5e-006   dvt0 = 1 dvt1 = 2
+dvt2 = 0 dvt0w   = 0 dvt1w   = 0 dvt2w   = 0
+dsub = 0.1   minv = 0.05   voffl   = 0 dvtp0   = 1e-011
+dvtp1   = 0.1   lpe0 = 0 lpeb = 0 xj   = 7.2e-009
+ngate   = 1e+023   ndep = 5.5e+018   nsd   = 2e+020   phin = 0
+cdsc = 0 cdscb   = 0 cdscd   = 0 cit   = 0
+voff = -0.13   nfactor = 2.3   eta0 = 0.004   etab = 0
+vfb   = -0.55   u0   = 0.04   ua   = 6e-010   ub   = 1.2e-018
+uc   = 0 vsat = 250000   a0   = 1 ags   = 0
+a1   = 0 a2   = 1 b0   = 0 b1   = 0
+keta = 0.04   dwg   = 0 dwb   = 0 pclm = 0.02
+pdiblc1 = 0.001   pdiblc2 = 0.001   pdiblcb = -0.005   drout   = 0.5
+pvag = 1e-020   delta   = 0.01   pscbe1   = 8.14e+008   pscbe2   = 1e-007
+fprout   = 0.2   pdits   = 0.01   pditsd   = 0.23   pditsl   = 2300000
+rsh   = 5 rdsw = 145   rsw   = 75   rdw   = 75
+rdswmin = 0 rdwmin   = 0 rswmin   = 0 prwg = 0
+prwb = 0 wr   = 1 alpha0   = 0.074   alpha1   = 0.005
+beta0   = 30   agidl   = 0.0002   bgidl   = 2.1e+009 cgidl   = 0.0002
+egidl   = 0.8   aigbacc = 0.012   bigbacc = 0.0028   cigbacc = 0.002
+nigbacc = 1 aigbinv = 0.014   bigbinv = 0.004   cigbinv = 0.004

```
+eigbinv = 1.1        nigbinv = 3 aigc = 0.0213        bigc = 0.0025889
+cigc = 0.002        aigsd   = 0.0213        bigsd   = 0.0025889        cigsd   = 0.002
+nigc = 1 poxedge = 1 pigcd      = 1 ntox = 1
+xrcrg1    = 12        xrcrg2   = 5
+cgso = 6.5e-011    cgdo = 6.5e-011   cgbo = 2.56e-011        cgdl = 2.653e-010
+cgsl = 2.653e-010    ckappas = 0.03    ckappad = 0.03    acde = 1
+moin = 15        noff = 0.9      voffcv   = 0.02
+kt1 = -0.11        kt1l = 0 kt2   = 0.022        ute   = -1.5
+ua1   = 4.31e-009      ub1   = 7.61e-018      uc1   = -5.6e-011        prt   = 0
+at     = 33000
+fnoimod = 1 tnoimod = 0
+jss   = 0.0001        jsws = 1e-011        jswgs     = 1e-010        njs   = 1
+ijthsfwd= 0.01      ijthsrev= 0.001        bvs   = 10        xjbvs     = 1
+jsd   = 0.0001        jswd = 1e-011        jswgd     = 1e-010        njd   = 1
+ijthdfwd= 0.01      ijthdrev= 0.001        bvd   = 10        xjbvd     = 1
+pbs   = 1 cjs   = 0.0005        mjs   = 0.5        pbsws     = 1
+cjsws     = 5e-010        mjsws     = 0.33        pbswgs     = 1 cjswgs   = 3e-010
+mjswgs   = 0.33        pbd   = 1 cjd   = 0.0005        mjd   = 0.5
+pbswd     = 1 cjswd     = 5e-010        mjswd     = 0.33        pbswgd   = 1
+cjswgd   = 5e-010        mjswgd   = 0.33        tpb   = 0.005        tcj   = 0.001
+tpbsw     = 0.005        tcjsw   = 0.001        tpbswg   = 0.005        tcjswg   = 0.001
+xtis = 3 xtid = 3

+dmcg = 0 dmci = 0 dmdg = 0 dmcgt      = 0
+dwj   = 0 xgw   = 0 xgl   = 0
+rshg = 0.4        gbmin     = 1e-010        rbpb = 5 rbpd = 15
+rbps = 15        rbdb = 15        rbsb = 15        ngcon     = 1
```

References

1. Berger, H.H.; Wiedmann, S.K. Complementary transistor circuit for carrying out Boolean functions. US Patent 3 956 641, May 1976.

2. Cai, J.; Ning, T.H.; D'Emic, C.; Chan, K.K.; Haensch, W.E.; Yau, J.-B.; Park, D.-G. Complementary thin-base symmetric lateral bipolar transistor on SOI, in Proc. of International Electron Device Meeting, Washington, D.C, USA, 2011, pp. 386-389, 10.1109/IEDM.2011.6131565.

3. Ning, T.H.; Cai, J. On the performance and scaling of symmetric lateral bipolar transistors on SOI. *IEEE J. of The Electron Device Society*, **2013**, 1, pp. 21-27, 10.1109/JEDS.2012.2233272

4. Cai, J.; Ning, T.H.; D'Emic, C.; Yau, J.-B.; Chan, K.K.; Yoon, J.; Jenkins, K.A.; Muralidhar, R.; Park, D.-G. SOI lateral bipolar transistor with drive current > 3 mA/μm, in Proc. of 2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, Monterey, USA, 2013, pp. 386-389, 10.1109/S3S.2013.6716518.

5. Cai, J.; Ning, T.H.; D'Emic, C.; Yau, J.-B.; Chan, K.K.; Yoon, J.; Muralidhar, R.; Park, D.-G. On the device design and drive-current capability of SOI lateral bipolar transistors. *IEEE J. of The Electron Device Society*, **2014**, 2, pp. 105-113, 10.1109/JEDS.2014.2331053.

6. Ning, T.H. A perspective on SOI symmetric lateral bipolar transistors for ultra-low-power systems. *IEEE J. of The Electron Device Society*, **2016**, 5, pp. 227-235, 10.1109/JEDS.2016.2528119.

7. Ning, T.H.; Cai, J. A Perspective on symmetric lateral bipolar transistors on SOI as a complementary bipolar logic technology, *IEEE J. of the Electron Devices Society*, **2015**, 1, pp. 24-36, 10.1109/JEDS.2014.2361696.

8. Maly, W.; Singh, N.; Chen, Z.; Li, X.; Pfitzner, A.; Kasprowicz, D.; Kuzmicz, W.; Lin, Y.-W.; Marek-Sadowska, M. Twin gate, vertical slit FET (VeSFET) for highly periodic layout and 3D integration, in Proc. 18th Int. Conf. MIXDES, 2011, pp. 145–150.

9. Kuzmicz, W.; Mierzwinski, P. A compact model of VES-BJT device, in Proc. 20th Int. Conf. MIXDES, Gdynia, Poland, 2013; pp. 96-100.

10. Mierzwiński, P.; Kuzmicz, W.; Domański, K.; Tomaszewski, D.; Głuszko, G. Bipolar transistor in VESTIC technology: prototype. *Proc. SPIE*, **2016**, 10175, pp. 101750E-1-101750E-9, 10.1117/12.2260787.

11. Sahu, A.; Bramhane, L.K.; Singh, J.; Symmetric lateral doping-free BJT: A novel design for mixed signal applications. *IEEE Trans. Electron Dev.*, **2016**, 7, pp. 2684-2690, 10.1109/TED.2016.2564701.

12. Sahu, A.; Kumar, A.; Tiwari, S.P. Performance investigation of universal gates and ring oscillator using doping- free bipolar junction transistor, in Proc. 2020 IEEE Silicon Nanoelectronics Workshop, Honolulu, USA, 2020, pp. 125-126, 10.1109/SNW50361.2020.9131668.

13. Beloni Devi, L.; Singh, K.; Srivastava, A. Study of substrate bias effect in symmetric lateral bipolar nano scale transistor on SOI for mixed signal applications, in Proc. 12th IEEE Int. Conf. on Nano/Micro Engineered and Molecular Systems, Los Angeles, USA, 2017, pp. 673-676, 10.1109/NEMS.2017.8017110.

14. Predictive technology models. Available online: http://ptm.asu.edu/ (accessed on 23 Nov. 2021)