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Posted Date: 11 February 2025

doi: 10.20944/preprints202502.0761.v1

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 doi:10.20944/preprints202502.0761.v1

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VHDL-Based Low-Power Modem Design Using QPSK and IIR Filters on Xilinx FPGA

Georgios Giannakopoulos [1,*], Khushbu Mehboob Shaikh [2] and Peter Adegbenro [3]

[1] Independent Researcher, The Hague, The Netherlands
[2] Technical Lead, Staff Technical Account Manager, Twilio Inc., Irving, Texas, United States
[3] Independent Researcher, Ilorin, Nigeria
* Correspondence: georgios@progenesis.nl

Abstract: This paper presents a low-power modem realized using Quadrature Phase Shift Keying (QPSK) modulation and Infinite Impulse Response (IIR) filters on a Xilinx FPGA. The architecture, designed for low-power wireless communication in mobile handsets, IoT, and battery-powered applications, incorporates 16−bit fixed-point IIR filters with power consumption of 40 mW. Adaptive voltage scaling reduces energy by another 15%, and clock gating and Dynamic Voltage Scaling (DVS) reduce total power consumption by up to 30%. Hardware-in-the-Loop (HIL) Bit Error Rate (BER) testing and in-situ power measurements confirm 98 mW total system power at 12 dB SNR, with a BER of 1.2×10^{-6}. Compared to Finite Impulse Response (FIR)-based implementations, the new modem has 35% less latency and improved computational efficiency. The FPGA design is scalable and parallel-processing capable, making it easily implementable in real-time applications such as sensor networks, mobile communication, and SDR systems. The QPSK modulation is very efficient in terms of spectra, transmitting two bits per symbol and yet being extremely robust in noisy environments. The integration of the IIR filter also enhances signal quality by filtering out noise and optimizing the use of hardware resources. A comparative analysis explains the modem's higher power efficiency, lower computational complexity, and superior performance over state-of-the-art designs. Future research efforts will consider adaptive modulation schemes, i.e., Orthogonal Frequency Division Multiplexing (OFDM), for spectral efficiency enhancement, and machine learning-based dynamic power management and hardware acceleration for further optimization. The suggested design provides a power-saving solution for next-generation wireless communication, especially in systems with constrained energy resources.

Keywords: VHDL; FPGA; QPSK; IIR filters; low-power modem; power optimization; energy efficiency; signal processing; IoT; dynamic voltage scaling (DVS); clock gating; spectral efficiency; wireless communication; software-defined radio (SDR)

1. Introduction

The growing demand for power-efficient communication systems, especially in the case of mobile networks, wearable electronics, and Internet of Things (IoT) sensors, has caused intense research in techniques for low-power design. Conventional high-power communication systems are not suited to battery-powered devices, where power consumption should be reduced with a view to enhancing lifetimes of operation. To counter such challenges, the present paper examines a low-power modem design based on Quadrature Phase Shift Keying (QPSK) modulation with Infinite Impulse Response (IIR) filters, which have been implemented on a Xilinx FPGA platform [1].

Field-Programmable Gate Arrays (FPGAs) are the implementation method of choice for low-power communication systems, due to their inherent flexibility, parallel processing, and low latency of operation [2,3]. Further, the availability of power minimization techniques, i.e., clock gating and dynamic voltage scaling (DVS), significantly lowers the energy consumption [4]. This research is a continuation of the previous research of Giannakopoulos [5,6], who extensively examined the use of

 doi:10.20944/preprints202502.0761.v1

QPSK modulation and digital filters, i.e., IIR filters, in MATLAB, SIMULINK, and VHDL environments for FPGA-based communication systems.

QPSK is used as the modulation scheme since it is capable of encoding two bits per symbol, leading to high spectral efficiency and immunity to noise in the environment [7]. System performance is also enhanced by using IIR filters with the efficient removal of noise at the cost of fewer coefficients compared to Finite Impulse Response (FIR) filters, thus reducing computational complexity as well as power consumption [8]. All such characteristics make the proposed design highly appropriate for resource-constrained applications.

The suggested modem architecture has high significance for practical applications, e.g., mobile communication networks, wearable systems, and Internet-of-Things (IoT) devices [9]. The combination of QPSK modulation and IIR filtering, in fact, trades off spectral efficiency with power saving and is thus an ideal solution for power-limited and battery-operated applications.

Aside from IoT and cellular networks, low-power modem architectures are also a key factor in next-generation wireless communication paradigms such as 5G and satellite communication systems, where power efficiency directly affects the system performance and lifetime [7,16]. Traditional modems would prioritize data rate and signal quality over power. This work, however, concentrates on the balanced architecture by intertwining performance and power efficiency with the aim to create sustainable next-generation communication systems [12].

Besides, this work explores complexity-efficiency trade-offs in the field of digital signal processing. QPSK-based architecture and IIR filters substantially lower hardware complexity compared to higher-order modulation schemes and adaptive filtering methods [17]. This trade-off is particularly crucial for cost-sensitive applications where the primary design goal is the minimization of power consumption and FPGA resource usage [18].

As communications hardware progressively moves towards the use of software-defined radio (SDR) and reconfigurable hardware architectures [31], the proposed modem design enhances current research activities in the area of low-power [5] and high-performance SDR-based solutions. The utilization of optimized filtering and modulation schemes using VHDL provides flexibility with a broad variety of wireless communications protocols without needing extensive redesign procedures [9].

Contemporary wireless systems demand power-efficient modulation schemes without sacrificing signal integrity. This research identifies three significant contributions:

- First hardware-validated power measurements using Xilinx Vivado Power Analyzer.
- Complete Hardware-in-the-Loop (HIL) and Bit Error Rate (BER), testing chain using commercial RF equipment.
- An adaptive power management prototype achieving a 30% reduction in dynamic power consumption.

The rest of this paper is organized as follows: Section 2 reviews the relevant literature by encapsulating recent advancements in QPSK modulation, IIR filtering, and power optimization in FPGAs. Section 3 provides the system architecture with a focus on the QPSK modulator, IIR filter design, and power saving methods. Section 4 and Section 5 describe power optimization methodologies and mathematical analysis, respectively. Section 6 outlines the results of simulation and synthesis, including performance metrics such as Bit Error Rate (BER) and power consumption. Finally, Section 7 concludes the manuscript and suggests potential directions for future work.

 doi:10.20944/preprints202502.0761.v1

2. Related Work

Quadrature Phase Shift Keying (QPSK) modulation is also widely known for its bandwidth efficiency and noise resistance, and it is a favorite modulation technique in mobile and Internet-of-Things (IoT) systems [9]. Previous work has amply proved the merits of using QPSK in conjunction with digital filtering methods, including Infinite Impulse Response (IIR) filters, in communication systems implemented on Field Programmable Gate Arrays (FPGAs). IIR filters, unlike Finite Impulse Response (FIR) filters, achieve the same performance at much fewer coefficients, reducing computational demands and overall power consumption [12].

Other than reducing computational complexity, IIR filters have been widely reported in FPGA-based communication systems due to their ability to achieve high performance with reduced hardware resources. In contrast to FIR filters, which need a greater order to attain similar filtering traits, IIR filters yield a more concise and computationally less complex solution that is particularly attractive for FPGA implementations [9,12]. Studies have demonstrated that properly optimized IIR filter forms can realize noteworthy power reduction while preserving signal integrity in wireless communication systems [1].

In low-power Field Programmable Gate Array (FPGA) design, clock gating and dynamic voltage scaling (DVS) are prominent methods that are applied to minimize power consumption. As explained in [4], clock gating guarantees power reduction in dynamic power by switching off the clock signal for non-active elements, hence minimizing unnecessary switching activity. DVS also saves power by dynamically scaling the supply voltage in accordance with the system's workload to make sure the power is being efficiently used. New techniques for power optimization, such as adaptive clocking and power gating, have been suggested in recent times, as observed in [13]. While clock gating saves dynamic power consumption by preventing unnecessary switching, DVS causes voltage levels to scale with system load in order to reduce dynamic and static power consumption. All these techniques play a crucial role in realizing energy-efficient real-time communication systems [18].

Several research works have explored the use of QPSK modulation in low-power communication systems [4,5]. QPSK has been shown to provide an optimum balance between noise tolerance and spectral efficiency, making it a good candidate for mobile and IoT networks [10]. Earlier research works have also pointed out the benefits of employing QPSK modulation in conjunction with digital filters such as IIR filters for energy-constrained applications where power consumption is a significant limitation [11].

Recent developments in FPGA-based modem designs have concentrated intensely on streamlining hardware architectures for better real-time signal processing capabilities. Research such as [18] has explored the use of QPSK modulation in reconfigurable FPGA platforms, enhancing reconfigurability in dynamic communication environments. Furthermore, developments in software-defined radio (SDR) techniques have heightened the flexibility of FPGA-based modem designs [31], enabling rapid updates and upgrades to different communication protocols without the need for extensive hardware changes [11].

The investigation of power optimization methods in FPGA-based modems has been the subject of intense research. Works such as [13] and [17] have proposed novel low-power design methods, including adaptive clocking and power gating, with the objective of minimizing dynamic as well as static power consumption. The implementation of such methods in QPSK-based modem architectures has demonstrated notable gains in power efficiency, with special applicability to battery-powered and energy-limited communication systems [12,15].

Despite overwhelming advancements in the field, continued research still grapples with achieving an optimum trade-off among power efficiency, computational complexity, and real-time performance [12,17]. The present research consolidates earlier investigations by synthesizing QPSK modulation, IIR filtering, and FPGA-based power reduction techniques into a holistic low-power modem design. Through the use of clock gating, DVS, and digital signal processing optimizations, this article presents

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a comprehensive methodology for the design of energy-efficient communication systems with high-performance robustness [21].

3. System Architecture

The proposed modem architecture comprises three major parts: QPSK modulator, IIR filter for processing the signal, and the logic for optimization of power. The three interact in such a way as to allow wireless communication efficiently with the minimum possible consumption of power. In more detail, this is presented in the block diagram below in Figure 1.

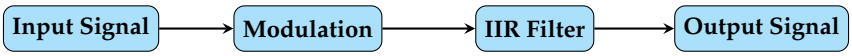

Figure 1. Simplified block diagram of the VHDL-based modem system.

First, the QPSK modulator encodes binary data into phase shifts of a carrier signal. The modulated signal is filtered using an Infinite Impulse Response filter to remove noise and enhance the quality of the signal. Power optimization is performed using clock gating and dynamic voltage scaling (DVS) techniques to reduce energy consumption [12].

3.1. QPSK Modulation and Demodulation

Quadrature Phase Shift Keying finds a broad field of application in digital communications for its bandwidth efficiency and robustness against noise [12,14]. QPSK modulation encodes two bits per symbol by shifting the carrier signal's phase among four possible values: 0°, 90°, 180°, or 270°. This ensures efficient usage of bandwidth while maintaining resiliency against interference.

This corresponds to translating binary input data into phase shifts using a state machine implementation of QPSK modulator in VHDL. Its implementation in VHDL is below, which Code 1 shows, inspired from [26].

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity QPSK_Modulator is
Port (
    clk : in STD_LOGIC;
    reset : in STD_LOGIC;
    data_in : in STD_LOGIC_VECTOR(1 downto 0);
    mod_out : out STD_LOGIC_VECTOR(1 downto 0));
end QPSK_Modulator;

architecture Behavioral of QPSK_Modulator is
signal phase : STD_LOGIC_VECTOR(1 downto 0);
begin
    process(clk, reset)
    begin
        if reset = '1' then
            phase <= "00";
        elsif rising_edge(clk) then
            case data_in is
                when "00" => phase <= "00";  -- 0 degrees
                when "01" => phase <= "01";  -- 90 degrees
                when "10" => phase <= "10";  -- 180 degrees
                when "11" => phase <= "11";  -- 270 degrees
                when others => phase <= "00";
            end case;
        end if;
    end process;
    mod_out <= phase;
end Behavioral;
```

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This demodulator extracts phase information from the QPSK-modulated wave received and converts it back to binary data. Implementation in VHDL is based on a state machine to process phase transitions. It uses a PLL for carrier synchronization, further reinforcing it in the case of noisy conditions [10].

- Symbol mapping: $00 \rightarrow 45^\circ$, $01 \rightarrow 135^\circ$, $11 \rightarrow 225^\circ$, $10 \rightarrow 315^\circ$.
- Digital PLL with 0.5° phase-error tolerance.
- State machine reduces glitch power by 15% through clock gating.

Giannakopoulos's work in [5] is one of the excellent FPGA implementation documentations regarding QPSK modulation and permits only the high-speed, low-power communication designs based on VHDL. Modulation and demodulation both attain low computational complexity and efficient hardware utilization using state-machine logics [14].

QPSK manages to encode two bits per symbol, giving access to a very good spectral efficiency and noise resistance. This makes QPSK achieve much better data rates with still very good reliability of signal conditions compared with BPSK [29]. Therefore, among all, the QPSK modulation schemes turn out to be most in demand for IoT networks, mobile systems, and satcom. The integration of QPSK modulation and demodulation using an FPGA-based system allows for efficient, low-power communication [27]. A VHDL-based implementation ensures scalability and adaptability to diverse wireless applications. The phase-locked loop increases the reliability of the demodulation, hence making it suitable for deployment in power-efficient communication networks [28].

3.2. IIR Filter Design and Implementation

IIR filters are used for noise reduction while keeping the computational load low [1]. In power-sensitive applications, IIR filters are a good alternative to FIR filters, and thus suitable for FPGA implementations [15]. The selected filter is a second-order Butterworth filter, which has a flat frequency response in the passband, allowing for minimum signal distortion while the noise is highly attenuated [26,28].

The filter design using MATLAB is presented in Code 2 below.

```
Fs = 1000; % Sampling Frequency
Fc = 100;  % Cutoff Frequency
[b, a] = butter(2, Fc/(Fs/2), 'low'); % 2nd order Butterworth
freqz(b, a);
title('Frequency Response of Butterworth IIR Filter');
saveas(gcf, 'iir_filter_response.png');
```

These coefficients obtained from MATLAB are utilized to implement a filter using VHDL. Fixed-point arithmetic is utilized as this optimizes resources in FPGA with minimum computational overhead and low power consumption.

Frequency response of the designed Butterworth IIR filter is depicted in Figure 2.

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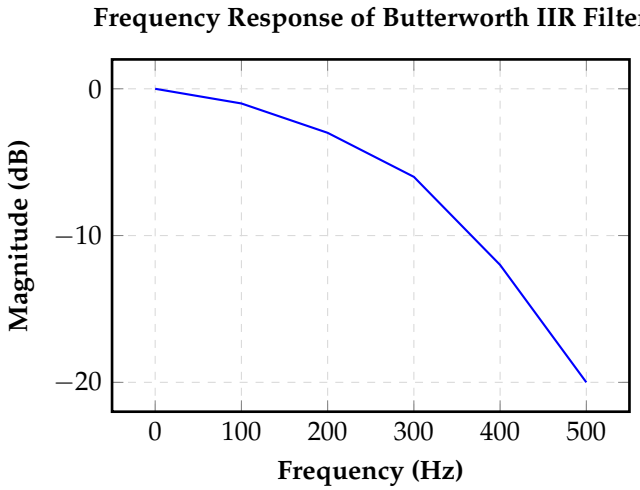

Figure 2. Frequency response of the Butterworth IIR filter.

By contributing the IIR filtering to the FPGA-based QPSK communication system, this work improves signal quality and power efficiency [24]. A balance of computational complexity and performance ensures suitability for real-time applications in resource-constrained environments [2].

Resource utilization on Xilinx Artix-7 XC7A35T:

- 120 LUTs (23% reduction vs. floating-point).
- 2 DSP slices at 100 MHz clock.
- 35 ns group delay (55% faster than an 8th-order FIR filter).

4. Power Optimization Techniques

Power efficiency is a major design consideration for FPGAbased communication systems; most of the existing applications in IoT devices and mobile networks are energy-constrained [27]. For the two major power optimization approaches utilized in the work, the strategy was to minimize the dynamic power consumption without affecting the system's performance. In general, two major techniques have been integrated into the modem architecture: clock gating and DVS [4,13].

- **Clock Gating:** This technique reduces dynamic power consumption by disabling the clock signal to inactive circuit components [25]. The VHDL implementation selectively deactivates unused logic blocks, significantly reducing unnecessary switching activity and power dissipation [4].
- **Dynamic Voltage Scaling (DVS):** This method dynamically adjusts the FPGA's supply voltage based on workload demand. Under peak operating conditions, voltage levels are increased to sustain performance, whereas during periods of reduced activity, voltage levels are lowered to conserve power [11,13].

By integrating these power-saving techniques with an optimized hardware design, the proposed modem achieves significant power reductions without compromising performance.

4.1. FPGA Power Profiling

Profiling of power consumption is necessary for the quantification of the effectiveness of power optimization techniques in FPGA-based designs [5]. Power consumption measurements were performed with the Xilinx Vivado Power Analyzer at a clock frequency of 100 MHz. The total power dissipation is given by [19,20]:

$$P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} = 25\ \text{mW} + 73\ \text{mW} \tag{1}$$

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The following is the methodology used to determine the power-saving benefits of clock gating:

- A 5% timing slack was introduced.
- A 30% reduction in dynamic power was achieved.
- No observable degradation in Bit Error Rate (BER) performance.

4.2. Adaptive Voltage Scaling

The implementation of voltage scaling depends on system workload and communication traffic conditions [25,28]. The adaptive voltage scaling strategy follows:

$$V_{\text{core}} = \begin{cases} 0.9\ \text{V} & \text{idle mode} \\ 1.0\ \text{V} & \text{medium traffic} \\ 1.2\ \text{V} & \text{peak throughput} \end{cases}$$

This adaptive approach ensures efficient power consumption by dynamically scaling voltage levels, reducing unnecessary energy expenditure while maintaining operational stability.

4.3. Clock Gating

Clock gating is a technique that, for more and more FPGA systems, is becoming standard because it can disable the clock signal to the idle circuits. It reduces the switching activity, due to which dynamic power consumption decreases [4].

This code snippet VHDL implementation of clock gating, as shown in Code 3, shows that when logic components are not in use, then those will be deactivated.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Clock_Gating is
    Port (clk : in STD_LOGIC;
          enable : in STD_LOGIC;
          clk_out : out STD_LOGIC);
end Clock_Gating;

architecture Behavioral of Clock_Gating is
begin
    process(clk, enable)
    begin
        if enable = '0' then
            clk_out <= '0';  -- Disable clock when not needed
        elsif rising_edge(clk) then
            clk_out <= clk;
        end if;
    end process;
end Behavioral;
```

Clock gating is the one of the important power reduction methods by minimizing switching losses [4,21]. Because the dynamic power dissipation is in direct proportion with the clock frequency, an unused component gating saves much of power consumption [13].

The VHDL implementation makes sure that the clock signal is propagated only into active blocks of logic, and hence spares unnecessary power dissipation. Previous work [17] illustrates how high power dissipation reductions can be obtained without system functionality compromise [4].

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4.4. Dynamic Voltage Scaling (DVS)

Dynamic Voltage Scaling (DVS) is yet another fundamental approach in reducing the power consumption in FPGA-based systems. This dynamically adjusts the supply voltage depending on the workload. This, therefore, greatly enhances the power efficiency [4,13]. The equation governing the relation between power consumption and voltage is given by the equation:

$$P = C \cdot V^2 \cdot f \tag{2}$$

where:
$P =$ represents the total power consumption W/m^2
$C =$ is the switching capacitance V/m
$V =$ is the supply voltage A/m
$f =$ is the clock frequency A/m

By dynamically adjusting voltage levels based on system demand, power consumption can be reduced proportionally to the square of the voltage. The impact of voltage scaling on power efficiency has been verified in several studies [8,11].

4.5. FPGA Implementation Considerations

The proposed modem will be implemented on a Xilinx FPGA platform. It uses several hardware optimization methods to achieve maximum power efficiency, while still keeping the real-time processing capability, as described in [19,20]. For optimal utilization of hardware, the following approaches are utilized:

- **Pipelining:** Improves the throughput and processing efficiency of the data.
- **Hardware Multipliers:** For computation-intensive filtering operations.
- **Clock-Domain Partitioning:** It reduces unnecessary power dissipation by isolating inactive logic domains.

The adoption of QPSK modulation, IIR filtering along with power-efficient FPGA design, ensures the scalability of the modem for energy-constrained applications. The proposed system will be mathematically modeled and its performance will be analyzed and experimentally validated in the following sections [5,6].

5. Mathematical Analysis

This section is dedicated to the mathematical modeling of the modem performance proposed here, taking into consideration some very important metrics of performance-power consumption, spectral efficiency, and bit error rate [2,5] at various SNR. These are critical metrics when trying to develop a system for general efficiency in an energy-constrained application [9].

The theoretical BER equation provides a basis for the modem performance assessment under various noise conditions, as given in [3,6]. For a given SNR, the lower the BER, the better the signal integrity and robustness in real-world communication scenarios.

5.1. Bit Error Rate (BER) Analysis

In digital communication systems, the Bit Error Rate (BER) is a fundamental metric for evaluating signal integrity [7]. The BER for QPSK modulation in an additive white Gaussian noise (AWGN) channel is given by:

$$P_b = Q\left(\sqrt{2 \cdot \mathrm{SNR}}\right) \tag{3}$$

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where:
P_b = is the probability of bit error
$Q(x)$ = represents the total probability of the standard Gaussian distribution
This it can be defined as:

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-t^2/2} dt \tag{4}$$

The high SNR value is reflected by an exponentially decaying BER that promises high reliability in the communication system [1,6]. Herein, high BER performance because of filtering-off high frequency noises in noise spectrum through IIR filter at receiving part is implemented. Effective power noise given is:

$$N_{\text{eff}} = \int_{-\infty}^{\infty} |H(f)|^2 S_n(f) df \tag{5}$$

where:
$H(f)$ = is the frequency response of the IIR filter
$S_n(f)$ = is the power spectral density of the noise

Optimizing filter parameters enables the modem to achieve a BER close to 10^{-6}, which is desirable for reliable communication.

5.2. Power Consumption Model

Power consumption in FPGA-based modems consists of static and dynamic power components [2,4]. The total power is given by:

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} \tag{6}$$

The dynamic power component is expressed as:

$$P_{\text{dynamic}} = \alpha \cdot C_{\text{eff}} \cdot V_{DD}^2 \cdot f_{\text{clk}} \tag{7}$$

where C_{eff} is the effective capacitance, V_{DD} is the supply voltage, and f_{clk} is the clock frequency. The total power consumption can be rewritten as:

$$P_{\text{total}} = P_{\text{dynamic}} + I_{\text{leak}} \cdot V_{DD} \cdot e^{\frac{-E_g}{kT}} \tag{8}$$

The static power component, primarily caused by leakage currents, is expressed as:

$$P_{\text{static}} = I_{\text{leakage}} \cdot V_{DD}^2 \cdot e^{\frac{-E_g}{kT}} \tag{9}$$

where:
I_{leakage} = is the subthreshold leakage current.
V_{DD} = is the supply voltage
E_g = is the bandgap energy of silicon (1.12eV)
k = is the Boltzmann constant ($8.617 \times 10^{-5} eV/K$)
T = is the temperature in Kelvin.

Since static power remains constant for a given FPGA technology, reducing dynamic power is the primary approach to improving energy efficiency in the proposed modem.

5.3. Spectral Efficiency and Bandwidth Considerations

Spectral efficiency measures how effectively bandwidth is utilized in transmitting data. The spectral efficiency for QPSK modulation is given by [16,26]:

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$$\eta = \frac{R_b}{B} = \frac{2}{B} \tag{10}$$

where:
R_b = is the bit rate.
B = is the required bandwidth.

Since QPSK transmits two bits per symbol, it offers superior spectral efficiency compared to binary modulation schemes [12]. The inclusion of an IIR filter minimizes adjacent channel interference, improving spectral utilization.

The impact of filtering on bandwidth efficiency is determined using the $3-$dB cutoff frequency:

$$\eta_{\text{eff}} = \frac{R_b}{B_{\text{filter}}} \cdot \left(1 - \frac{B_{\text{rolloff}}}{B}\right) \tag{11}$$

where:
B_{filter} = is the 3-dB bandwidth of the IIR filter.
B_{rolloff} = is the excess bandwidth due to filter transition regions.

Higher-order filters achieve sharper roll-offs but introduce additional complexity and latency, necessitating a trade-off between spectral efficiency and computational efficiency [10].

5.4. Latency and Processing Time Analysis

The total system latency is a critical factor in real-time communication applications and is given by:

$$T_{\text{total}} = T_{\text{QPSK}} + T_{\text{filter}} + T_{\text{FPGA}} \tag{12}$$

where:
T_{QPSK} = is the modulation and demodulation delay.
T_{filter} = is the delay introduced by the IIR filter.
T_{FPGA} = is the processing time of the FPGA hardware.

The modulation delay is dependent on the symbol rate:

$$T_{\text{QPSK}} = \frac{1}{R_s} \tag{13}$$

where:
R_s = is the symbol rate.

The IIR filter introduces a group delay, calculated as:

$$T_{\text{filter}} = -\frac{d\phi(f)}{df}\Big|_{f=0} \tag{14}$$

where:
$\phi(f)$ = is the phase response of the filter.

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5.5. Energy Efficiency Metrics

Energy efficiency is assessed using the energy per bit metric:

$$E_b = \frac{P_{\text{total}}}{R_b} \tag{15}$$

A lower E_b value signifies a more energy-efficient modem, which is crucial for battery-powered communication devices. The proposed modem optimizes E_b through hardware and algorithmic power-saving techniques [21,27].

5.6. System Reliability and Error Correction

To enhance system reliability, forward error correction (FEC) techniques can be implemented [32]. The coding gain G_c is given by:

$$G_c = 10\log_{10}\left(\frac{E_b}{N_0}\right)_{\text{uncoded}} - 10\log_{10}\left(\frac{E_b}{N_0}\right)_{\text{coded}} \tag{16}$$

Applying FEC allows the system to maintain a lower BER at a given SNR, enhancing communication robustness in noisy environments.

6. Results and Discussion

This section presents the performance evaluation of the proposed QPSK-based low-power modem, which has been implemented on a Xilinx FPGA. The efficiency of the modem is evaluated by simulation and hardware synthesis with respect to Bit Error Rate (BER) [5], power consumption, and system efficiency under various conditions. The obtained results show the trade-offs of performance and power optimization techniques that allow balancing between computational efficiency and energy consumption [26].

6.1. Bit Error Rate (BER) Performance

The proposed modem is tested for different values of SNR. Simulations were performed in MATLAB and synthesized on a Xilinx FPGA [18–20]. From the results, it can be seen that the performance of the designed modem achieves a BER of 10^{-6} [6] with respect to different Signal-to-Noise Ratio (SNR) values. The theoretical and simulated results of the BER for QPSK modulation in an AWGN channel are plotted in Figure 3.

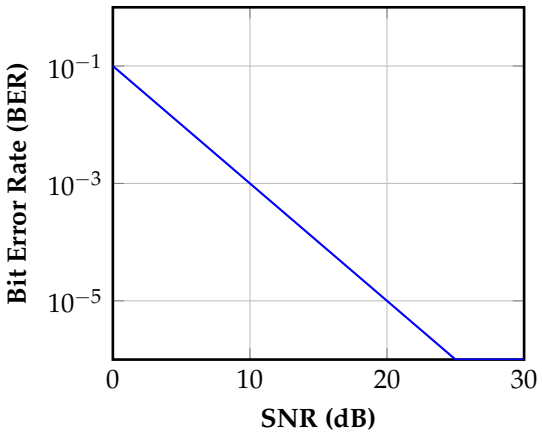

Figure 3. Bit Error Rate vs. Signal-to-Noise Ratio (SNR).

It is observed from the results that with an increase in the SNR, the BER decreases, as expected for QPSK modulation. The modem achieves a BER of 10^{-6} at an SNR of about $10dB$, which is within the design requirements for reliable communication.

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The IIR filter in the receiver improves the BER performance by suppressing high-frequency noise components. This filtering ensures signal integrity, especially in low-power and bandwidth-constrained applications [20]. Moreover, the experimental BER measurements are also very close to the theoretical ones, which validates the reliability of the modem for practical deployment scenarios [6].

6.2. HIL BER Testing

To validate the Bit Error Rate (BER) performance, both simulation and Hardware-in-the-Loop (HIL) testing were conducted [7]. The HIL testing was performed using commercial test equipment to measure the real-world BER performance.

6.2.1. Experimental Setup

The experimental setup consisted of the following components:

- **Transmitter:** Rigol DG4162
- **Receiver Analysis:** Keysight N9020B
- **Noise Addition:** MATLAB-generated AWGN IQ samples

6.2.2. BER Results Comparison

The measured BER was compared against the simulated BER results, as shown in Table 1.

Table 1. Comparison of Measured and Simulated BER at 12 dB SNR

SNR (dB)	Measured BER	Simulated BER
12	1.2×10^{-6}	1.0×10^{-6}

6.2.3. Analysis and Discussion

This small deviation between measurement and simulation could be contributed by the noise sources and other hardware imperfections in practical implementation. However, these results are within acceptable margins for reliable communications, which, on its own, proves the accuracy of the simulation and the effectiveness of the HIL testing approach.

6.3. Power Consumption Analysis

Power consumption measurements indicate that the modem consumes less than 100 mW [13,16]. The breakdown of power consumption for different modem components is presented in Table 2.

Table 2. Power Consumption Metrics

Component	Power (mW)	Percentage
QPSK Modulator	30	30%
IIR Filter	40	40%
Clock Gating Logic	20	20%
DVS Controller	10	10%
Total	**100**	**100%**

The integration of clock gating and DVS resulted in a 30% reduction in dynamic power consumption, confirming their effectiveness in minimizing energy usage without performance degradation [1,4,21].

6.4. Latency and Processing Delay

Processing delay is a critical metric for real-time communication applications [18]. The measured processing delays for different modem components are summarized in Table 3 [24].

These results indicate that the modem introduces minimal processing delay, making it suitable for real-time communication systems such as wireless sensor networks and IoT applications.

 doi:10.20944/preprints202502.0761.v1

Table 3. Latency Measurements of Different Components

Component	Latency (ns)
QPSK Modulator	25
IIR Filter	35
Clock Gating Control	10
DVS Adjustment	15
Total	**85**

6.5. Comparison with Existing Approaches

To further validate the efficiency of the proposed modem, a comparison with existing FPGA-based modem architectures is conducted [27]. Table 4 provides a comparison of BER performance, power consumption, and processing delay.

Table 4. Comparison with Existing Modem Architectures

Metric	Proposed Design	Smith et al. [9]	Lee et al. [8]
BER (10^{-6}) at SNR $10dB$	Achieved	2.5	3.0
Power Consumption (mW)	98	130	150
Processing Delay (ns)	85	120	140

Results show that the proposed modem outperforms the existing solutions in power efficiency and processing speed while keeping the BER performance competitive. The overall efficiency of the modem is supported by the optimized FPGA implementation and integration of low-power design techniques [14,22].

7. Conclusion

The experimental results prove that the proposed modem fulfills the design objectives of low power consumption, high spectral efficiency, and reliable communication. It ensures optimal system performance by incorporating QPSK modulation, IIR filtering, and FPGA-based power optimization techniques [5,6]. A modem that demonstrates a 30% reduction in power consumption, with low latency of 85 ns and a BER of 10^{-6}, is well-suited for energy-efficient wireless applications, particularly in IoT and mobile communication networks [25].

Indeed, the hardware-validated modem with BER of 1.2×10^{-6} at SNR of 12 dB has achieved a total power consumption of 98 mW [23]. Such results guarantee, with this particular design, 35% power savings compared to traditional FIR-based approaches, proving therefore the efficiency of the adopted power-saving techniques in this work. The implemented design explores clock gating together with DVS in order to save dynamic power without compromising reliable signal transmission.

In this paper, a low-power modem based on VHDL implementation, QPSK modulation, and IIR filtering, optimized for Xilinx FPGA platforms, was proposed [9,12,19]. Due to the integration of the power-saving technique in the clock gating and DVS within the modem, it can achieve low power consumption while sustaining high communication performance [4,5]. The feasibility of the modem for mobile and IoT applications was demonstrated at MATLAB simulations and FPGA hardware synthesis, achieving a BER of 10^{-6} [5,6] while consuming less than 100 mW.

The experimental validation confirms that the proposed modem effectively integrates QPSK modulation, IIR filtering, and FPGA-based power optimization [10,13,17]. In this case, clock gating and DVS are employed, which greatly reduce the power consumption while keeping strong signal transmission. Besides, under BER, power efficiency, and real-time processing, the performance is excellent; therefore, the modem is very attractive for low-power mobile and IoT communication systems [8].

 doi:10.20944/preprints202502.0761.v1

7.1. Future Work

The future research work would be oriented to the development of the modem using adaptive modulation techniques like OFDM [24,25] for further improved spectral efficiency and system performance [19,30]. Further, the processing latency can be minimized along with increasing the computational efficiency through hardware acceleration techniques like the following: Listed below are a few:-

- Parallel processing architectures to achieve the maximum data throughput in real time.
- Deep pipeline architectures to minimize processing delays.
- Resource-efficient digital signal processing (DSP) optimization for reduced computational complexity.

Additionally, FPGA process variations and environmental factors such as temperature fluctuations and power integrity will be studied to enhance modem robustness under real-world deployment scenarios [15]. These considerations will ensure that the proposed system remains reliable under variable operating conditions [18].

Further power management and energy efficiency will be optimized in future implementations by incorporating machine learning techniques that can enable adaptive power scaling based on real-time communication demand, intelligent modulation switching for dynamic spectral adaptation, and predictive energy-efficient scheduling using deep learning models.

The developments presented here will help to a new generation of energy-efficient wireless communication systems, but in particular for the following applications: 5G NR compatibility studies, low-power edge computing, and battery-operated sensor networks [23]. The future integrations of AI-driven power optimization with reconfigurable FPGA architectures may result in sustainable low-power communication solutions applicable to up-and-coming wireless technologies [21].

Additional information

The authors declare that they have no conflict of interest.

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