Article

Encapsulation of NEM Memory Switches for Monolithic-Three-Dimensional (M3D) CMOS-NEM Hybrid Circuits

Hyun Chan Jo and Woo Young Choi*

[1] Department of Electronics Engineering, Sogang University, Seoul, Republic of Korea; jhc10337@naver.com
* Correspondence: wchoi@sogang.ac.kr; Tel.: +82-2-715-8467

Abstract: Considering the isotropic release process of nanoelectromechanical systems (NEMS), defining the active region of NEM memory switches is one of the most challenging process technologies for the implementation of monolithic-three-dimensional (M3D) CMOS-NEM hybrid circuits. In this paper, we propose a novel encapsulation method of NEM memory switches. It uses alumina (Al_2O_3) passivation layers which are fully compatible with CMOS baseline process. The Al_2O_3 bottom passivation layer can protect intermetal dielectric (IMD) and metal interconnection layers from vapor hydrogen fluoride (HF) etch process. Thus, the controllable formation of the cavity for the mechanical movement of NEM memory switches can be achieved without causing any damage to CMOS baseline circuits as well as metal interconnection lines. As a result, NEM memory switches can be located in any places and metal layers of an M3D CMOS-NEM hybrid chip, which makes circuit design easier and more volume-efficient. The feasibility of our proposed method is verified based on experimental results.

Keywords: CMOS-NEMS; NEMS; NEM memory switch; encapsulation; M3D

1. Introduction

CMOS-nanoelectromechanical (CMOS-NEM) hybrid circuits have been researched intensively thanks to their unique advantages: low-power consumption, high performance, low fabrication cost and high chip density [1]-[7]. Some pioneering experimental results of CMOS-NEM hybrid circuits have been reported [2], [5]. They have NEM devices on the top of a chip or in CMOS back-end-of-line (BEOL) metal interconnection layers. For the implementation of monolithic-three-dimensional (M3D) CMOS-NEM hybrid circuits, the release process is important to form the atmospheric or vacuum environment for the mechanical operation of NEM memory switches [2]. Generally, the release process is performed by using vapor hydrogen fluoride (HF) etch. By using the vapor HF etching, the inter-metal-dielectric (IMD) layers such as the tetraethyl orthosilicate (TEOS) layers, which surround NEM memory switches, can be effectively removed with the high selectivity toward metal layers [8]. However, conventional release process using vapor HF etch can cause catastrophic influences on IMD and metal interconnection layers because it is an isotropic etching process: NEM memory switches and adjacent metal interconnection lines collapse due to the widespread removal of IMD layers. Thus, as shown in Figs. 1a and 1b, it is difficult to place the metal interconnection lines around NEM memory switches, which will be called "dead zone" in this manuscript. The existence of the dead zone makes M3D CMOS-NEM hybrid circuit design difficult and volume-inefficient.

To minimize the dead zone surrounding NEM memory switches, this manuscript proposes a novel CMOS-process-compatible encapsulation method as shown in Fig. 1c. In the proposed method, NEM memory switches are encapsulated by alumina (Al_2O_3) bottom/top passivation layers. The TEOS lower/upper sacrificial layers encapsulated by the Al_2O_3 bottom/top passivation layers are selectively removed by vapor HF etch while the rest of the regions are protected. Thus, the controllable formation of a cavity is feasible for the mechanical movement of the NEM memory switches without damaging CMOS baseline circuits and metal interconnect lines. From now, this cavity will be called "active region" of a NEM memory switch. To sum up, because our proposed

Peer-reviewed version available at Micromachines 2018, 9, 317; doi:10.3390/mi9070317

encapsulation method defines the active regions of NEM memory switches without generating dead zones, NEM memory switches can be placed in any metal interconnection layers. To confirm the proposed method, prototype encapsulated NEM memory switches are implemented.

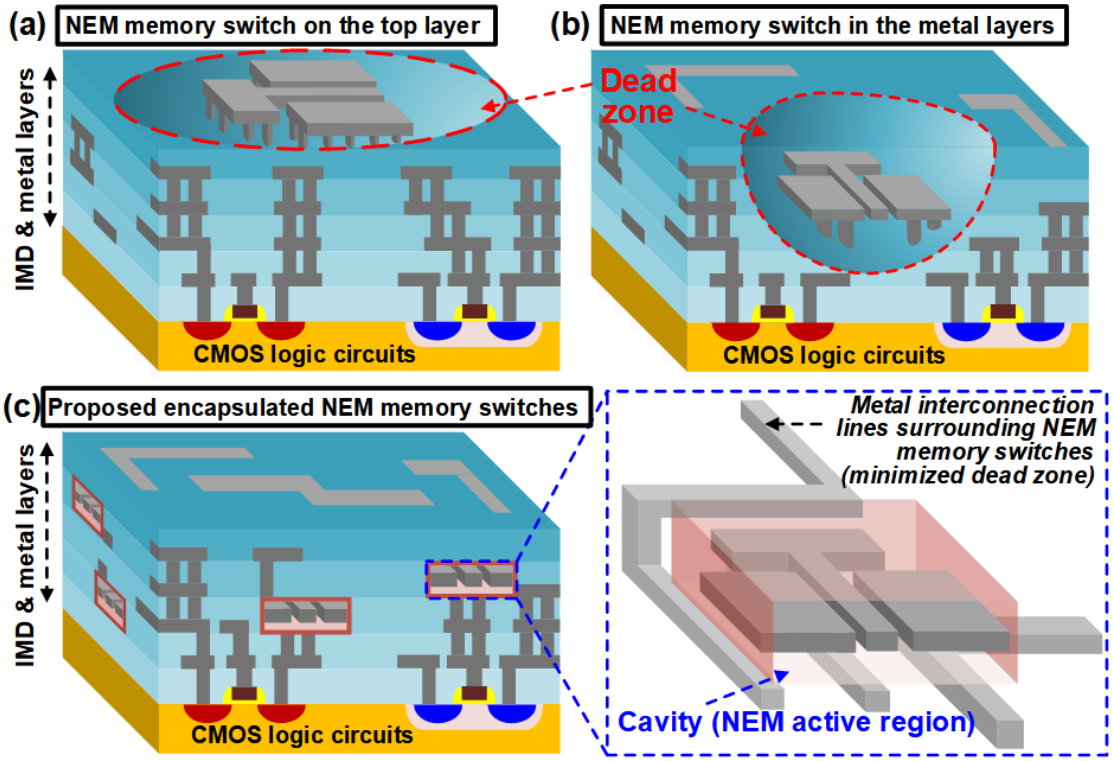

Figure 1. Conceptual views of (**a**) a NEM memory switch only on the top layer, (**b**) a NEM memory switch in the CMOS-BEOL metal layers and (**c**) the proposed encapsulated NEM memory switches for M3D CMOS-NEM hybrid circuits.

2. Encapsulation process

Fig. 2 shows the key process steps of the encapsulated NEM memory switches. First, a 50-nm-thick silicon dioxide (SiO_2) layer is grown by wet oxidation. Then, a 500-nm-thick aluminum (Al) layer is sputtered and patterned by inductively coupled plasma (ICP) etching. The Al patterns correspond to the metal interconnect lines of CMOS baseline circuits. Third, a 500-nm-thick TEOS IMD layer is deposited and patterned by plasma-enhanced chemical vapor deposition (PECVD) and magnetically-enhanced reactive ion etching (MERIE) process, respectively, to define the active regions of NEM memory switches. Subsequently, a 200-nm-thick Al_2O_3 bottom passivation layer is deposited by multi-sputtering process. The Al_2O_3 bottom passivation layer protects the metal interconnection lines and IMD layers from the following vapor HF etch [9]-[11]. Fifth, a 200-nm-thick TEOS layer is deposited as a lower sacrificial layer. Next, a 500-nm-thick Al layer is deposited and patterned to form NEM memory switches. During the patterning process, the 85-nm-wide airgap between the movable cantilever beam and selection lines of NEM memory switches is formed by focus ion beam (FIB) process while the rest of patterns are defined by a conventional stepper. Seventh, a 500-nm-thick TEOS layer is deposited and patterned as an upper sacrificial layer. It should be noted that the active regions of NEM memory switches are defined and filled by the lower and upper sacrificial layers. Eighth, a 200-nm-thick Al_2O_3 top passivation layer is deposited to encapsulate the active regions of NEM memory switches. Subsequently, small-sized etch holes are patterned on the Al_2O_3 top passivation layer by FIB process. Tenth, the lower and upper TEOS sacrificial layers are removed through the etch holes by vapor HF etch at 40 °C and 15 minutes. Finally, a thick TEOS IMD layer is deposited on the Al_2O_3 top passivation layer to form the cavity surrounding NEM memory

switches which acts as the active region. The encapsulated active regions are in the vacuum condition depending on TEOS deposition conditions. This encapsulation method is fully CMOS-process-compatible, which can be easily applied to the fabrication of M3D CMOS-NEM hybrid circuits.

For cavity formation, the etch holes should have the aspect ratio high enough to prevent TEOS from filling the cavity again through the etch holes. Fig. 3 shows scanning-electron-microscopy (SEM) cross-sectional images of etch holes. In order to form the etch holes with various aspect ratios, two FIB process conditions have been adjusted: beam current and target diameter. The aspect ratio of the etch holes in Figs. 3a and 3b are measured to be 0.79 (beam current = 50 pA and target diameter = 160 nm) and 1.01 (beam current = 10 pA and target diameter = 160 nm), respectively. It is interesting that two different layers are observed below the Al_2O_3 top passivation layer in those two cases. The former is a thin TEOS layer which is originated from the unwanted TEOS inflow through the etch holes. It is problematic in that it prevents the motion of a cantilever beam of a NEM memory switch. On the contrary, the latter results from the redeposition process during FIB sample cutting process for SEM measurment, which does not exist in the main samples [12]. Thus, to suppress TEOS inflow, the aspect ratio of the etch holes needs to be increased. If the aspect ratio is increased up to 1.14 (beam current = 10 pA and target diameter = 80 nm) as shown in Fig. 3c, no unwanted TEOS inflow is observed. Only, the redeposition layer originated from FIB sample cutting process is formed under the Al_2O_3 top passivation layer.

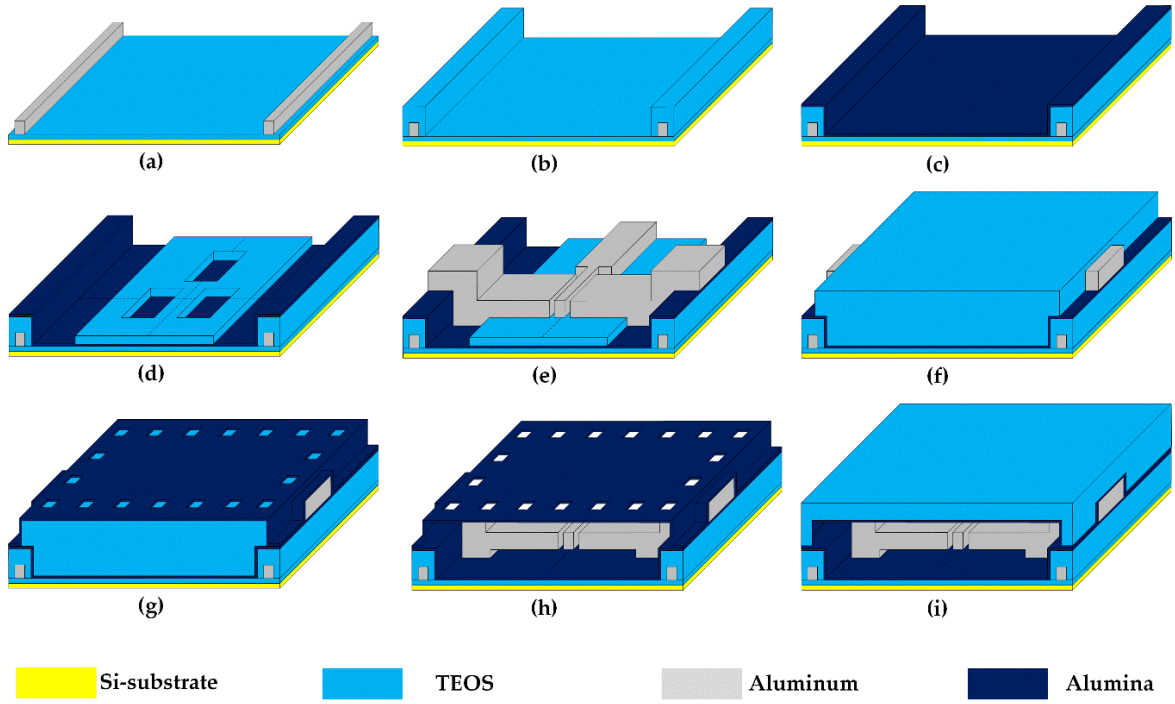

Figure 2. Key process steps of the encapsulated NEM memory switches. (**a**) Al deposition and patterning for the formation of metal interconnection lines. (b) TEOS deposition and patterning for IMD formation. (c) Al_2O_3 bottom passivation layer deposition. (d) Lower TEOS sacrificial layer deposition and patterning. (e) Al deposition and patterning for the formation of a NEM memory switch. (**f**) Upper TEOS sacrificial layer deposition and pattern. (g) Al_2O_3 top passivation layer deposition and etch hole formation. (h) Removal of the lower/upper sacrificial layers through etch holes by using vapor HF etch. (i) TEOS deposition for cavity sealing.

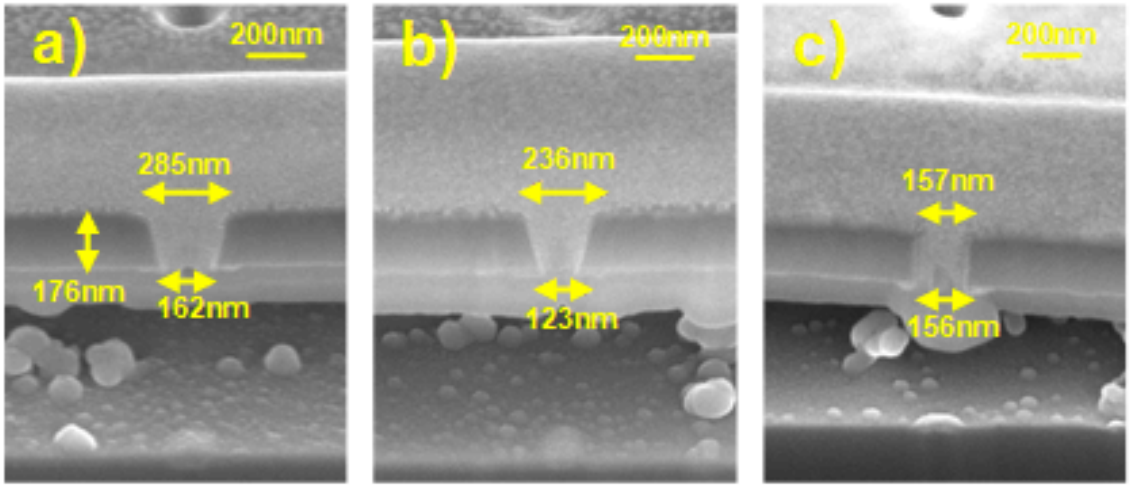

Figure 3. Cross-sectional SEM images of etch holes with the variation of the beam current and target diameter of FIB process. (a) Aspect ratio = 0.79 when beam current is 50 pA and target diameter is 160 nm. (b) Aspect ratio = 1.01 when beam current is 10 pA and target diameter is 160 nm. (c) Aspect ratio = 1.14 when beam current is 10 pA and target diameter is 80 nm.

3. Results and Discussion

Fig. 4 shows the SEM images of the fabricated NEM memory switch encapsulated in a cavity. Figs. 4a-4c and 4d-4f show the NEM memory switches before and after vapor HF etch, respectively. The active region of the encapsulated NEM memory switch is formed well next to the metal interconnection lines as shown in Fig. 4. Figs. 4b and 4c confirm that Al_2O_3 top and bottom passivation layers wrap the NEM memory switch and lower/upper TEOS sacrificial layers. Figs. 4d-4f show that the TEOS lower/upper sacrificial layers are successfully removed by vapor HF etching. In Fig. 4e, it is confirmed that the sacrificial layers are completely removed by vapor HF without damaging the cavity regions. This forms the active region of NEM memory switch, allowing activation between metal layers. Especially, Fig. 4e shows that the NEM memory switch is successfully fabricated in the cavity. On the other hand, Fig. 4f shows that the IMD layer out of the cavity is also removed by vapor HF etch, which means that the Al_2O_3 bottom passivation layer fails to protect the IMD layer from vapor HF etch. It is because vapor HF can penetrate into the Al_2O_3 layer following grain boundaries if the Al_2O_3 layer is formed by sputtering process. Thus, in order to increase the film density of the Al_2O_3 passivation layer, atomic layer deposition (ALD) process is used rather than sputtering process. Figs. 5a-5d show the transmission electron microscopy (TEM) images of test sample using a 20-nm-thick ALD-deposited Al_2O_3 layer before and after 1-, 5-, 15-mimute vapor HF etch at 40 ˚C, respectively. As predicted, it is observed that the SiO_2 IMD layer is completely protected passivated by the ALD-deposited Al_2O_3 layer.

Fig. 6 shows the current-*vs*.-voltage curves of the fabricated NEM memory switch encapsulated in a cavity. It shows the reasonable nonvolatile switching operation between selection line 1 (L_1) and selection line 2 (L_2). The endurance cycle number is ~ 11 times due to the weak mechanical property of aluminum. In the first switching operation, the voltage difference between the movable cantilever beam and L_1 (V_{L1}) becomes higher than the pull-in voltage ($V_{pull\text{-}in}$) and then the movable cantilever beam is stuck onto L_1, which is called State 1. In this case, because the adhesion force (F_{ad}) is larger than the restoring spring force of the movable cantilever beam (F_r), the movable beam remains in contact with L_1 even when V_{L1} is 0 V [13]. Thus, the nonvolatile data signal storage can be achieved. In the second switching operation, the voltage difference between the movable cantilever beam and L_2 (V_{L2}) becomes higher than the switching voltage (V_{swit}) and then the location of the beam tip is changed from L_1 to L_2, which is called State 2. During the measurement, maximum current level was limited to suppress micro-welding effects. Poor endurance cycle number can be improved by downscaling the dimension of NEM memory switches and changing beam materials [14], [15].

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 30 May 2018 doi:10.20944/preprints201805.0454.v1

Peer-reviewed version available at Micromachines 2018, 9, 317; doi:10.3390/mi9070317

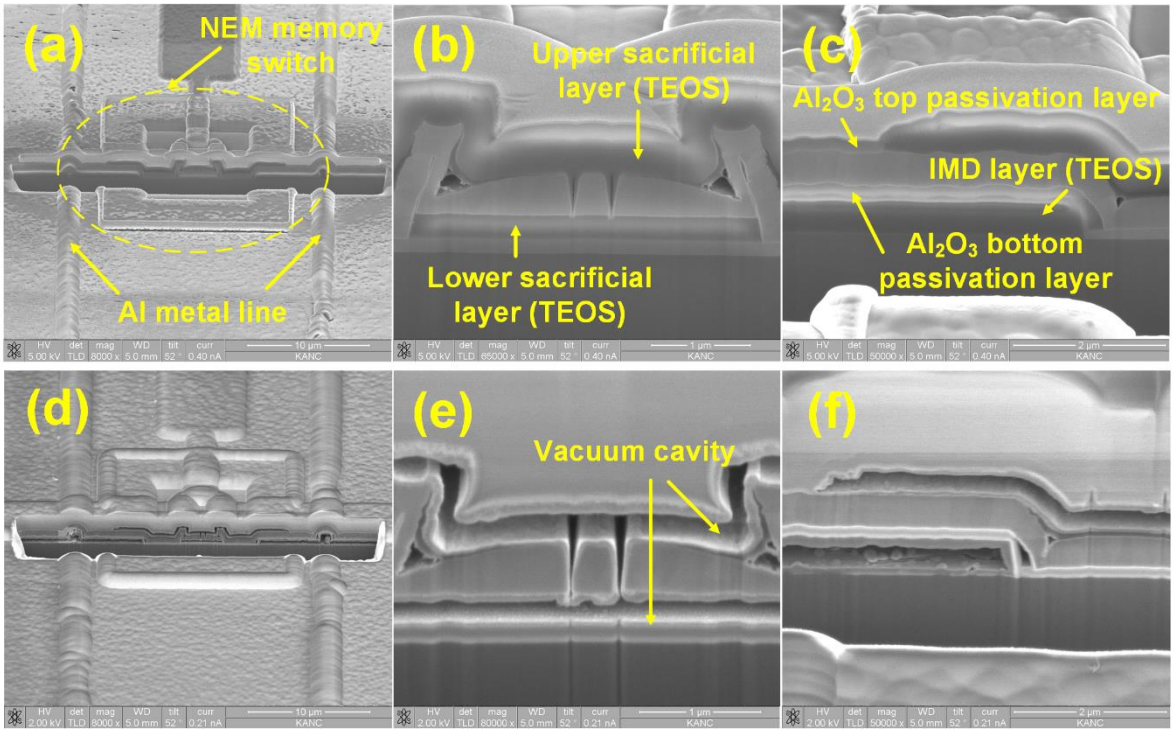

Figure 4. (a) NEM memory switch and metal interconnection lines, (b) NEM memory switch and (c) metal interconnection lines before vapor HF etch. (d) NEM memory switch and metal interconnection lines, (e) NEM memory switch and (f) metal interconnection lines after vapor HF etch.

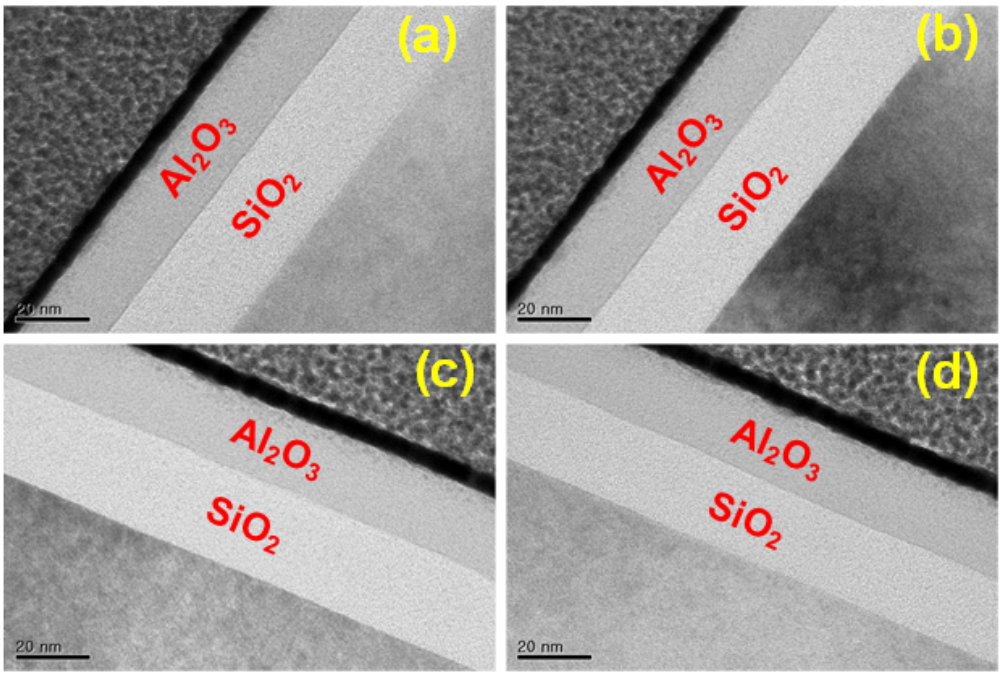

Figure 5. TEM images of an ALD-deposited Al_2O_3 layer (a) before and after (b) 1-minute, (c) 5-minute and (d) 15-minute vapor HF etch.

Peer-reviewed version available at Micromachines 2018, 9, 317; doi:10.3390/mi9070317

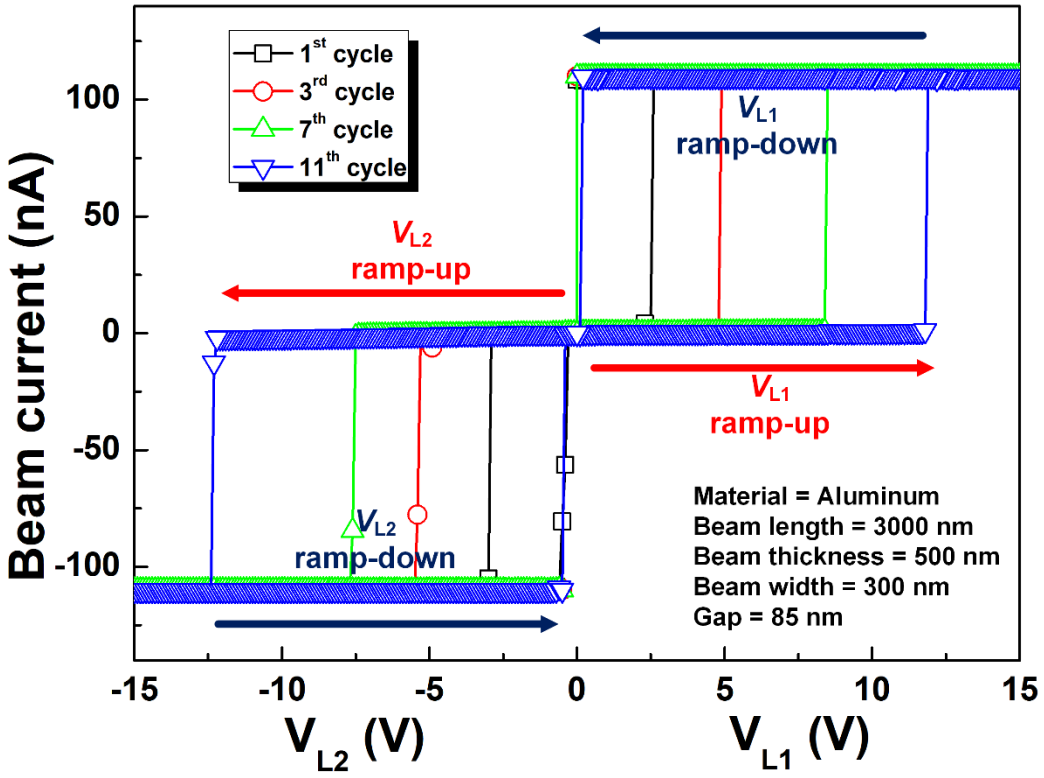

Figure 6. Current-*vs*.-voltage curves of the fabricated NEM memory switch encapsulated in a cavity.

4. Conclusions

In this work, a fabrication method to Encapsulation NEM memory switch for CMOS-NEM hybrid circuits is proposed by using commercial CMOS process and materials. Specification of the stable encapsulated NEM memory switch is successfully confirmed based on the prototype fabrication and measurement results. By applying the proposed process confirmed in this work, the controllable formation for the cavity for mechanical movement of the NEM devices can be achieved without damaging the CMOS device as well as the metal interconnect lines. As a result, The NEM device is free in the entire area of the chip and exists in various layers, so that it can be easily designed in a circuits. Therefore, the proposed fabrication process can lay the groundwork for commercialization of the CMOS-NEM hybrid circuits

Acknowledgments: This work was supported in part by the Sogang University Research Grant of 2017(201710129.02), in prat by the NRF of Korea funded by the MSIP under Grant NRF-2018R1A2A2A05019651 (Mid-Career Researcher Program), NRF-2015M3A7B7046617 (Fundamental Technology Program), NRF-2016M3A7B4909668 (Nano-Material Technology Development Program) and in part by the MOTIE/KSRC under Grant 10080575 (Future Semiconductor Device Technology Development Program).

Author Contributions: Woo Young Choi conceived and designed the experiments. Hyun Chan Jo performed the experiments. Both of the authors analyzed the data and wrote the paper.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Kim, Y.J.; Choi, W.Y. Three-Dimensional Integration of Complementary Metal-Oxide-Semiconductor-Nanoelectromechanical Hybrid Reconfigurable Circuits. *IEEE Electron Device Lett.* **2015**, *36*, 887-889.
2. Kwon. H.S.; Kim. S.K.; Choi, W.Y.; Monolithic Three-Dimensional 65-nm CMOS-Nanoelectromechanical Reconfigurable Logic for Sub- 1.2-V Operation. IEEE Electron Device Lett. **2017**, *38*, 1317-1320
3. Dong, C.; Chen. C.; Mitra. S.; Chen. D. Architecture and Performance Evaluation of 3D CMOS-NEM FPGA. *System Level Interconnect Prediction Workshop (SLIP)*, **2011**, 2
4. Chong, S.; Lee, B.G.; Parizi, K.B.; Provine, J.; Mitra, S.; Howe, R.T.; Wong, P. Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit. In Proceeding of the 2011 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 5-7 December 2011; pp. 1-4.
5. Muñoz-Gamarra, J.; Uranga, A.; Barniol, N. CMOS-NEMS Copper Switches Monolithically Integrated Using a 65nm CMOS Technology. Micromachines, **2016**, 1-7.
6. Muñoz-Gamarra, J.; Alcaine, P.; Marigó, E.; Giner, J.; Uranga, A; Esteve, J.; Barniol, N. Integration of NEMS resonators in a 65nm CMOS Technology. *Microelectron. Eng*. **2013**, *110*, 246-249.
7. Riverola, M.; Vidal-Alvarez, G.; Torres, F.; Barinol, N. 3-Terminal Tungsten CMOS-NEM Relay. Proceeding of PH. D. Research in Microelectronics and Electronics (PRIME) of Conference On 2014 10th, Grenoble, France, 30 June -3 July 2014; pp. 1-4.
8. Magis, T.; Ballerand, S.; Comte, B.; Pollet, O. Deep Silicon Etch for Biology MEMS Fabrication: Review of Process Parameters Influence versus Chip Design. *SPIE MOEMS-MEMS, International Society for Optics and Photonics*, **2013**, 826120A.
9. Witvrouw, A.; Bois, B.D.; Moor, P.D.; Verbist, A.; Hoof, C. V.; Bender, H.; Baert, C. Comparison between Wet HF Etching and Vapor HF Etching for Sacrificial Oxide removal. *Micromachining and Microfabrication. International Society for Optics and Photonics*, **2000**, 130-141.
10. Williams, K.R.; Gupta, K.; Wasilik, M. Etch Rate for Micromachining Processing-Part Ⅱ. *Journal of Micromechanical Systems*, **2003**, *12*, 761-778
11. Bakke, T.; Schmidt, J. Friedrichs, M.; Völker, B. Etch Stop Materials for release by vapor HF etching. Proceeding of MicroMechanics Europe Workshop (MME) of conference 2005, Göteborg, Sweden, 109-106.
12. Winter, D.A.M.; Mulders, J.J.L. Redeposition Characteristics of Focus Ion Beam Milling for Nanofabricaiton. *Journal of Vacuum Science Technology B*, **2007**, *28*, 2215-2218
13. Soon, B.W.; Ng, E.J.; Qian, Y.; Singh, N.; Tsai, M.J.; Lee, C.K. A Bi-stable Nanoelectromechanical Nonvolatile memory based on van der Waals force. *Appl. Phys. Lett*. **2013**, *103*, 053122.
14. Choi, W.Y.; Osabe, T.; Liu, T.J.K. Nano-electro-mechanical nonvolatile memory (NEMory) cell design and scailing. *IEEE Trans. Electron Devices*, **2008**, *55*, 3482-3488.
15. Lee. H.M.; Choi W.Y.; Switching voltage modeling of nano-electromechanical (NEM) memory switches. Proceeding of 24th Korean Conf. Semiconductors (KCS). Hongcheon, Korea, 13-15 February 2017; pp. 32