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Article

Improvement of Electrical Performance in P-Channel LTPS Thin-Film Transistor with a-Si:H Surface Passivation

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Abstract: We report the effects of surface passivation by depositing a hydrogenated amorphous silicon (a-Si:H) layer on the electrical characteristics of low temperature polycrystalline silicon thin film transistors (LTPS TFTs). The a-Si:H layer was optimized by hydrogen dilution and its structural and electrical characteristics were investigated. The a-Si:H layer in the transition region between a-Si:H and μc-Si:H resulted in superior device characteristics. Using an a-Si:H passivation layer, the field-effect mobility of the LTPS TFT was increased by 78.4% compared with a conventional LTPS TFT. Moreover, the leakage current measured at a V_{GS} of 5 V was suppressed because the defect sites at the poly-Si grain boundaries were well passivated. Our passivation layer, which allows thorough control of the crystallinity and passivation-quality, should be considered a candidate for high performance LTPS TFTs.

Keywords: poly-Si TFT; FT-IR, Raman, surface passivation; leakage current

1. Introduction

Currently, the display industry has been widely investigating was to meet new market demands for low-cost, large-size, high-resolution, high-frame-rate, and 3D displays. Thin film transistors (TFTs) as switching or driving devices are one of the most important components. Low temperature polycrystalline silicon (LTPS) TFTs have been widely used because their field effect mobility is higher than that of hydrogenated amorphous silicon (a-Si:H) TFTs, so that high resolution displays with ultra-high densities (3840 × 2160, UHD) can be fabricated. Because poly-Si TFTs are very robust under electrical and optical stress, they can be used in various applications [1]. However, there are crucial disadvantages of LTPS TFTs, such as high off-state leakage currents originating from defects in the grain boundaries of poly-Si [2]. To reduce leakage currents in poly-Si TFTs, some additional structures have been proposed including lightly doped drain (LDD) and offset gate structures [3]. However, these structures require additional processing and costs, so they have not been fully applied in the display industry. To reduce the off-state leakage current, Kim et al. proposed a simple method based on the insertion of a thin (10 nm) a-Si:H layer [4]. They explained the reason for the reduced leakage current using an energy band diagram and the current paths in the LTPS TFT with an a-Si:H passivation layer and a larger band gap. Inserting a larger band gap material between the active layer and gate insulator can result in a reduced rate of thermionic emission. Thus, the minimum leakage current was successfully reduced and the on/off ratio was improved. However, the field-effect mobility (12 $cm^2/V{\cdot}s$) of the LTPS TFT with an a-Si:H passivation layer was remarkably lower than that of a TFT without an a-Si:H passivation layer (58.3 $cm^2/V{\cdot}s$). Although they solved the leakage current problem in LTPS TFTs through the simple insertion of passivation layer with a larger band gap, the field-effect mobility was severely decreased, so that the high performance of poly-Si TFTs disappeared.

In this work, we investigated the reduction of leakage current without sacrificing the field-effect mobility. We tried depositing an a-Si:H passivation layer on the poly-Si layer. An a-Si:H passivation layer has been used to achieve a high conversion efficiency in hetero junction solar cells [5-6]. However, the use of an a-Si:H passivation layer in poly-Si TFTs has so far not been reported. The optimized a-Si:H layer passivates dangling bonds at the interface and reduces carrier recombination, thus improving the device characteristics. We investigated the deposition of an a-Si:H passivation layer and optimized the dilution gas ratio. Different a-Si:H layers were deposited using different gas ratios of SiH_4:H_2, and the characteristics of the a-Si:H layers were evaluated by Raman spectroscopy, Fourier transform infrared spectroscopy (FT-IR), and quasi-steady-state photoconductance (QSSPC) measurements to examine their crystallinity (X_C), defects, bonding, and passivation-quality. Finally, LTPS TFTs with different passivation layers were fabricated and their electrical performance was evaluated. The leakage current was successfully reduced without sacrificing the field-effect mobility by using an optimized a-Si:H layer.

2. Device fabrication

A 50-nm-thick a-Si:H film was deposited on the 300-nm-thick buffer oxide layer by plasma enhanced chemical vapor deposition (PECVD). The a-Si:H layer was dehydrogenated at 400 °C in a N_2 atmosphere for 10 minutes and then crystallized using a XeCl (308 nm) excimer laser. After the formation of LTPS, the a-Si:H passivation layer was deposited on the LTPS. To investigate the effect of surface passivation on the electrical performance of LTPS TFTs, the 10-nm-thick passivation layers were deposited by PECVD using different silane (SiH_4) and hydrogen (H_2) gas flow rates. Various dilution gases, such as helium (He) and hydrogen, have already been studied for the deposition of a-Si:H [7]. The layer of a-Si:H deposited using He as a dilution gas was found to contain disordered and loose networks. However, the a-Si:H deposited with H_2 dilution gas was found to form a more dense structure, so we used H_2 as the dilution gas in this work. The SiH_4 flow rate was varied from 20 sccm to 6 sccm and the H_2 flow rate was varied from 20 sccm to 36 sccm. The gas ratio (GR) of H_2 / (SiH_4 + H_2) was changed from 0.50 to 0.86, while the plasma power density was fixed at 1.27 W/cm^2. The highest and lowest deposition rates of a-Si:H passivation layers were 2.59 nm/min at GR of 0.75 and 0.55 nm/min at GR of 0.5, respectively. The 220-nm-thick SiO_2 gate insulator was deposited on the passivation layer. An aluminium layer was deposited on the gate insulator to serve as the gate metal, and then the substrate was patterned. Source and drain doping with boron was performed using an ion shower. Then, the source and drain regions were activated at 400 °C in a N_2 atmosphere for 4 hours. The channel width and length of the fabricated TFTs were 180 and 50 μm, respectively. The electrical characteristics of the LTPS TFTs with different passivation layers were examined using a semiconductor parameter analyser at room temperature under dark conditions. To further understand the passivation layer's structural and electrical characteristics, Raman spectroscopy, FTIR, and QSSPC measurements were conducted.

3. Results and Discussion

Raman spectroscopy is a well-known technique for distinguishing the structural characteristics of thin films. In particular, it can indicate the ordering of an amorphous silicon film. The defects of a-Si:H are mainly detected at low frequency (300 cm^{-1} ~ 400 cm^{-1}). We investigated the use of Raman spectroscopy for evaluating the passivation layer. Fig. 1 shows the Raman spectra of passivation layers deposited using different GR values. The 100-nm-thick passivation layer was deposited on a glass substrate. The measured Raman spectra were decomposed into several gaussian component peaks located at around 150, 300, 410, and 480 cm^{-1}, corresponding to the transverse acoustic (TA), longitudinal acoustic (LA), longitudinal optical (LO), and transverse optical (TO) modes [8-10]. The Raman characteristics of the passivation layers were strongly influenced by the GR. When the GR was increased from 0.5 to 0.75, the ratios of TA/TO, LA/TO and LO/TO were reduced. When the GR was over 0.75, the ratios of TA/TO, LA/TO, and LO/TO rapidly increased. The increase of TA/TO, LA/TO, and LO/TO has been related to the enhanced generation of defects in passivation layers [8-10]. The inset shows the ratios of TA/TO, LA/TO, and LO/TO at different GR values. Furthermore,

the crystallinity (X_C) of the passivation layer was calculated using the Raman peak ratio of the broad band at 480 cm^{-1} (a-Si:H) and the strong band at 520 cm^{-1} (c-Si). A Raman spectrum characteristic of μc-Si:H was observed at GR values above 0.75 and the X_C sharply increased.

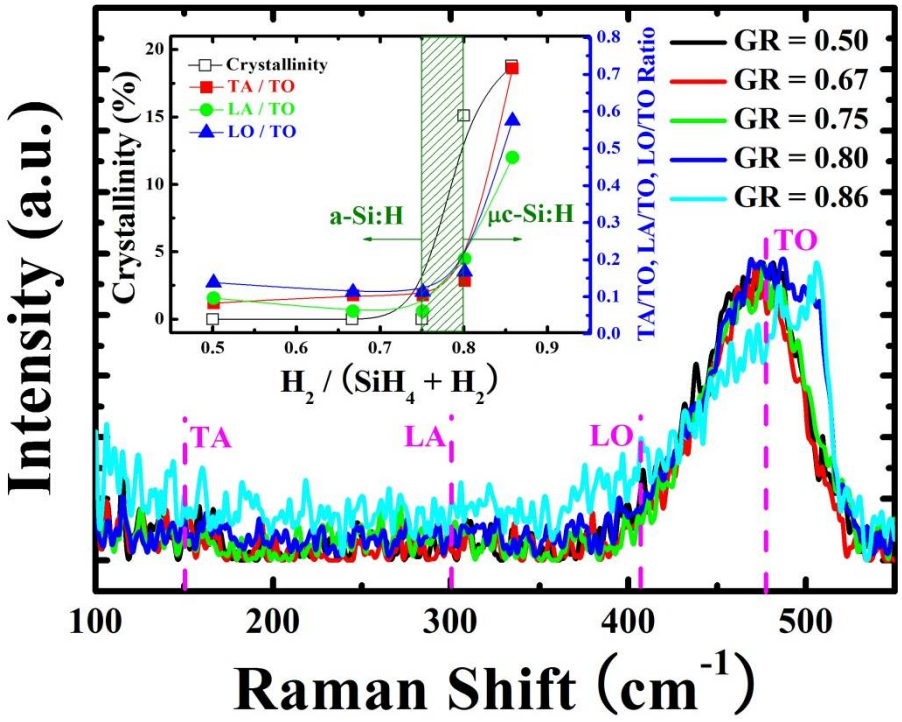
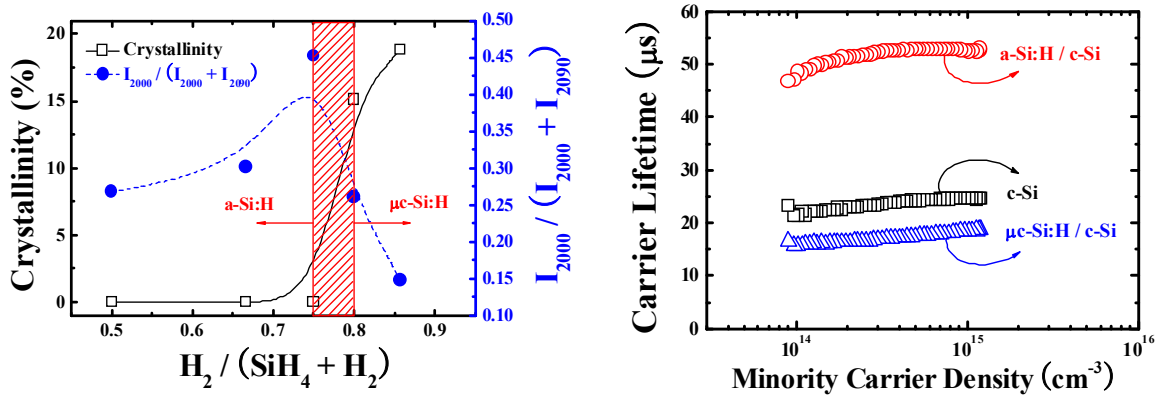


Fig. 1. The Raman spectra of passivation layers as a function of GR. The inset shows the dependence of the Raman characteristic parameters and crystallinity on GR.

To further understand the silicon hydrogen bonds, we performed FT-IR measurements, which can easily detect the incorporation of Si and H. To analyze the FT-IR spectra, a 100-nm-thick passivation layer was deposited on c-Si. Fig. 2(a) shows the microstructure parameter (R*) of the passivation layers deposited by at different GR values. The FT-IR absorption of a-Si:H and μc-Si:H provides specific information about the type of bonds present between Si and H [11-12]. In this study, two kinds of bonds with a stretching vibrational mode were observed to investigate the structural properties of the passivation layers, such as Si-H bonds with a peak at around 2000 cm^{-1} and $Si=H_2$ bonds with a peak at around 2090 cm^{-1}. As the GR was increased to 0.75, I_{2000} also increased. But, I_{2000} decreased for GR values over 0.8. For calculating the properties of the passivation layer, the quantity R* was introduced. R* was defined as $I_{2000} / (I_{2000} + I_{2090})$. The $Si=H_2$ bonding factor representing the quality of layer was regarded as a measure of defects or voids. As $Si=H_2$ bonding increased, many defects remained in the thin film. The R* value gradually increased from 0.27 at a GR of 0.5 to 0.45 at a GR of 0.75 and sharply decreased to 0.15 at a GR of 0.86. Based on the correlation with Raman results, the highest R* value and the transition region from a-Si:H to μc-Si:H were well matched.

To investigate the passivation ability of different passivation layers, QSSPC measurements were conducted for a-Si:H on a single crystalline silicon wafer (c-Si) (a-Si:H/c-Si), μc-Si:H on c-Si (μc-Si:H/c-Si), and a pure c-Si sample. Fig. 2(b) shows the carrier lifetime characteristics of the passivation layers formed using different $H_2 / (SiH_4 + H_2)$ gas ratios. This measurement is widely used in the contactless characterization of solar cells. Many thin films such as a-Si:H and Al_2O_3 have been employed to passivate the interface or bulk defects [13-14]. The system is based on a radio frequency bridge with an inductive coil that generates electromagnetic fields in the wafer. The interfaces of a silicon substrate represent a severe discontinuity in its crystalline structure. The poly-Si, especially at the interface, has many dangling bonds, so that a large density of defect levels

could be found within the bandgap near the interface. By using an appropriate surface passivation layer, such as an optimized a-Si:H film, these dangling bonds in poly-Si grain boundaries could be passivated, thus reducing the interface trap state [15]. Flash lamp was irradiated on semiconductor surface. The excessive electron and hole pairs were generated, and then generated carriers were decayed. The minority carrier lifetime, τ can be considered as the amount of time carriers remain at defect sites of the Si surface. Because the τ of a thin film could be dominantly influenced by surface conditioning, it can be useful for evaluating the passivation quality. In this study, a c-Si substrate without a passivation layer was used as a reference with a τ value of 22.23 μs. The τ of a-Si:H/c-Si with a GR of 0.75 was highest at 51.77 μs and the τ of μc-Si:H/c-Si with a GR over 0.75 was reduced below the reference τ. By using the optimized a-Si:H (GR=0.75) passivation layer, the lowest interface trapped charge density was expected.



(a) (b)

Fig. 2. The characteristics of the passivation layers as function of GR. (a) The calculated crystallinity by Raman spectroscopy and microstructure by FT-IR (b) Carrier lifetime characteristics of passivation layers.

Fig. 3 shows the electrical properties obtained from transfer curves of the p-channel LTPS TFTs with and without passivation layers on the poly-Si layer. The width and length of the p-channel poly-Si TFTs were 180 μm and 50 μm, respectively (width/length = 3.6). The transfer curves were measured at a drain bias of -0.1 V. The extracted electrical properties of the p-channel LTPS TFTs with and without passivation layers are displayed in Table I. The field effect mobility (μ) was calculated by the maximum transconductance method at V_{DS} = -0.1 V and the threshold voltage was observed at the (Width/Length) × V_{GS} at drain current density of 10 nA. The leakage current ($I_{D.Leakage}$) was measured at a V_{GS} of 5 V. The LTPS TFT without a passivation layer had the following electrical properties: μ of 49.58 $cm^2/V{\cdot}s$, subthreshold swing (S.S.) of 0.91V/dec, and the $I_{D.Leakage}$ of 7.62×10^{-11} A/cm^2. When the GR was 0.75, the LTPS TFT with a passivation layer exhibited a μ of 88.53 $cm^2/V{\cdot}s$, S.S of 0.58V/dec and $I_{D.Leakage}$ of 2.46×10^{-12} A/cm^2. Moreover, the threshold voltage was considerably reduced. These improved TFT characteristics were attributed to the fact that the optimized a-Si:H layer can easily passivate the poly-Si interface with a high trap density. Especially, it is known that the improved threshold voltage (V_{TH}) and S.S. are related to deep defect states. The characteristics of poly-Si TFTs fabricated at low temperature are dominated by interface and grain boundary defect states. It is clear that the amount of trap states between the poly-Si layer and the gate oxide layer was reduced due to the optimized a-Si:H layer, as proven by FT-IR and QSSPC measurements. The leakage current was also reduced by the passivation layer. Significant band-bending occurs between the channel and drain region because of the reversely biased p-n junction, where the leakage current can flow via the defect sites at the poly-Si grain boundary [16]. The optimized passivation layer was effective at reducing the number of such defect sites. To express this numerically, the interface defect sites between SiO_2 and poly-Si were estimated by the Levison and Proano method [17-18]. The number of defect sites can be expressed as

$$N_T = [\left(\frac{S.S.}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1)](\frac{C_{ox}}{q}) \quad (1)$$

where S.S. is subthreshold swing, q is unit charge, T is absolute temperature, and C_{ox} is the capacitance of the gate oxide.

The number of interface defect sites was successfully reduced by using a passivation layer. But, the on characteristics were quite different. In the case of LTPS TFTs with μc-Si:H passivation layers, the electrical properties were degraded with a higher S.S and a lower field-effect mobility. The most likely reason for this degradation is the creation of new dangling bonds on the poly-Si layer by highly diluted hydrogen. Our passivation process can supply additional hydrogen for the passivation, but it could also create new dangling bonds [19]. Therefore, the dilution gas ratio for the passivation layer was carefully controlled to avoid creating new dangling bonds.

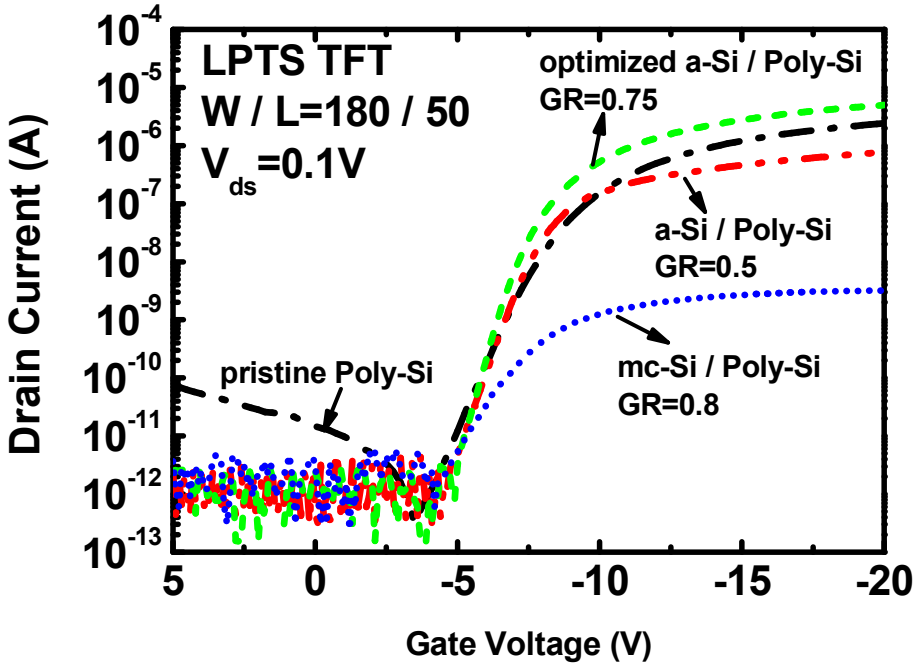


Fig. 3. Transfer characteristics of LTPS TFTs with and without passivation layers.

Table 1. Comparison of electrical characteristics of p-channel LTPS TFTs with and without passivation layers on glass substrates.

Parameter	Without passivation layer	With passivation layer		
		a-Si:H (GR=0.5)	Opt. a-Si:H (GR=0.75)	μc-Si:H (GR=0.8)
μ (cm²/Vs)	49.58	18.2	88.53	1.3
S.S. (V/dec)	0.91	0.72	0.58	1.19
N_T (cm^{-2})	7.38×10^{12}	5.50×10^{12}	4.61×10^{12}	1.01×10^{13}
V_{TH} (V)	-6.75	-6	-5.9	-6.4
$I_{d.leak}$ (A/cm²)	7.62×10^{-11}	2.3×10^{-12}	2.46×10^{-12}	3.68×10^{-12}

Fig. 4 shows a schematic diagram of the energy bands of p-channel LTPS TFTs with and without passivation layers under negative and positive gate bias based on the energy band

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difference, defect density, and current paths. When a negative gate voltage was applied to the LTPS TFTs, the energy band diagram is represented in Fig. 4(a) for 'only poly-Si', (b) 'a-Si:H/poly-Si', and (c) μc-Si:H/poly-Si. Compared to the diagram in (a), the a-Si:H/poly-Si layers resulted in a bandgap difference between a-Si:H (E_g=1.88eV) and poly-Si (E_g=1.12eV), and the channel carrier mobility was enhanced due to the improved interface quality. In the case of μc-Si:H (E_g=1.2eV) /poly-Si, the effect of this bandgap difference was smaller and resulting in degraded interface quality. When the gate voltage is positive, the energy band diagram can be represented as in Fig. 4 (d) for 'only poly-Si', (e) 'a-Si:H/poly-Si', and (f) μc-Si:H/poly-Si. In the case of (d), when the gate voltage was positive, the carriers flowed from the drain to the source via poly-Si. In the case of the poly-Si with a passivation layer, when the gate voltage was positive, the carriers flowed from the drain to the source via the passivation layer and/or passivation layer/poly-Si/buffer. The field emission, denoted by path C, for the SiO_2/poly-Si TFT was suppressed by the presence of a wide band gap passivation. Therefore, the dominant current path may be A or B as depicted in Fig. 4(d), (e) and (f). Path A represents the thermionic field emission in the passivation region and path B represents the thermionic field emission in the poly-Si due to the weakened electric field in the poly-Si due to the presence of the passivation layer.

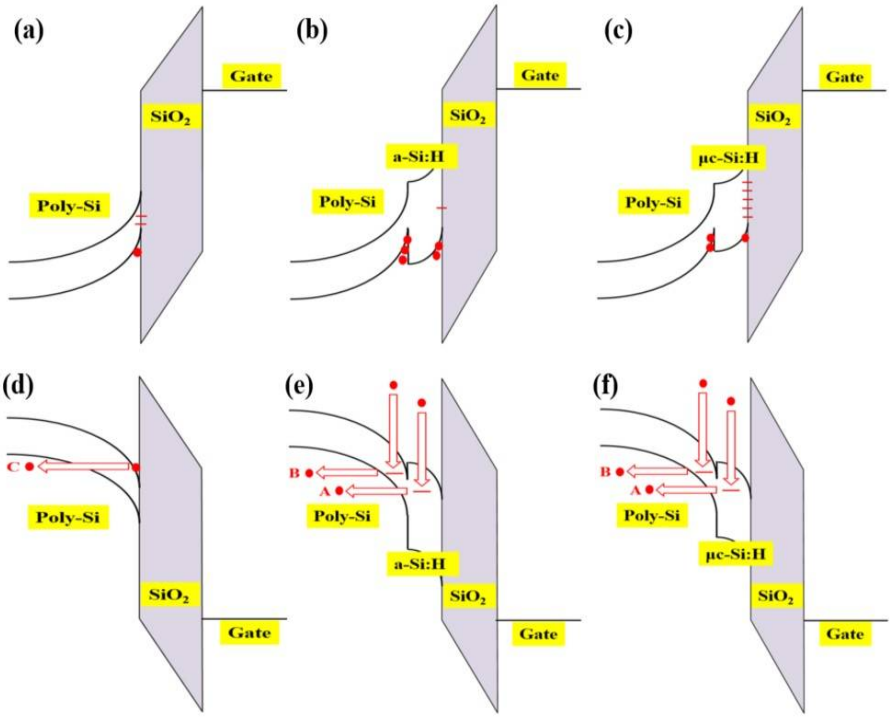

Fig. 4. The schematic energy band diagram of p-channel LTPS TFTs with and without passivation layers under negative and positive gate bias based on the energy band difference, defect density, and current paths. (a) Only poly-Si under negative gate bias, (b) a-Si:H/poly-Si under negative gate bias, (c) μc-Si:H/poly-Si under negative gate bias, (d) only poly-Si under positive gate bias, (e) a-Si:H/poly-Si under positive gate bias, and (f) μc-Si:H/poly-Si under positive gate bias.

4. Conclusions

We fabricated p-channel LTPS TFTs with a a-Si:H passivation layer to reduce the leakage current without sacrificing field effect mobility. Poly-Si TFTs have excellent and reliable electrical reliable characteristics, but they still suffer from leakage currents under off state bias. To suppress the leakage current, many techniques have been tried, but they were frustrated a field effect mobility reduction. In this work, we proposed a new method, which was the insertion of a thin a-Si:H passivation layer on the poly-Si with a wide band gap and high passivation-quality on the

LTPS layer. The a-Si passivation layer was optimized by controlling the dilution gas ratio and its structural and electrical characteristics were reported. The on state and off state characteristics of the poly-Si TFTs with an optimized a-Si:H passivation layer were considerably improved because the defect sites at the poly-Si grain boundaries were well passivated. Based on the findings of this study, the use of passivation layer with high passivation-quality and a large band gap should be considered as potential candidates for high performance LTPS TFTs.

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