Role of structure and composition on the performances of p-type tin oxide thin-film transistors processed at low-temperatures

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Abstract: This work reports the role of structure and composition on the determination of the performances of p-type SnOx TFTs deposited by rf magnetron sputtering at room temperature, followed by a post-annealed step up to 200ºC at different oxygen partial pressures (Opp), between 0% and 20%, but where the p-type conduction was only observed between 2.8-3.8%. The role of structure and composition were evaluated by XRD and Mössbauer spectroscopic studies. The study allows to identify the best phases/compositions and thicknesses (around 12 nm) to be used that lead to the production of TFTs with a bottom gate configuration, on glasses coated with conductive Indium Tin Oxide, followed by Aluminium Titanium Oxide dielectric layer with saturation mobility of 4.6 $cm^2V^{-1}s^{-1}$ and on-off ratio above 7×10^4, operating at the enhancement mode with a saturation voltage of -10 V.

Keywords: p-type TFT, p-type oxide semiconductors, SnO electrical properties; Oxide structure analysis

1. Introduction

Oxide electronics or in more generic terms transparent electronics, is emerging as an appropriate alternative to amorphous silicon (a-Si:H) and organic semiconductors, especially for thin film transistors (TFTs) and more complex electronic circuits. Oxide semiconductors are a promising class of TFT materials that have made impressive demonstration in display applications in a relatively short time, challenging silicon in the flexible electronics field. Although some initial attempts during the 60s were done for SnO_2,[1] and ZnO,[2] TFT channel layers, only forty five years later, with the work of Hosono,[3] Wager,[4] Carcia,[5] and Fortunato,[6] a significant worldwide interest appeared, especially for active matrix for organic light emitting diodes (AMOLED) technology, both in industry and academia. Oxide semiconductors have unique electronic properties like high mobility irrespective to the structure nature and excellent uniformity and homogeneity in device parameters associated to a low or room temperature deposition process allowing the use of low cost and flexible substrates such as polymer or even paper.[7]

However, there is no report on p-type oxide TFTs with performance similar to n- type, which is mainly limited by the low hole mobilities.[8] Achieving high performance p-type oxide TFTs will definitely promote a new era for electronics in rigid and flexible substrates, away from silicon. Moreover, it will shape the electronics of tomorrow by allowing the production of complementary metal oxide semiconductors (CMOS), a key device to fuel the microelectronics revolution in the so-

called technologies of information and communication, by allowing the use of highly compact circuits with low power consumption.

At present, almost all reported oxide TFTs are based on n-channel devices.[1-9] The carrier conduction path (valence band) in p- type oxides is mainly formed from the oxygen *p* asymmetric orbitals, which severely limit the carrier mobility and lead to poor TFT performance. Cu_2O is a p-type oxide with mobility exceeding 100 $cm^2V^{-1}s^{-1}$.[10,11] However, TFTs prepared from Cu_2O have field-effect mobilities and on-off current ratio below 1 $cm^2V^{-1}s^{-1}$ and 10^2 respectively, due to difficulty in controlling the hole density in channel layer.[11-13] While conventional passive applications require the maximum possible hole density for optimal conductivity, the channel layer requires a low hole density in order to modulate the channel conductance by an applied electric field. Most of organic TFTs reported in the literature are p-type.[14,15] Even though organic TFTs have been the topic of intense research for the past few decades, the overall performance is still poor compared to oxide TFTs, namely low mobilities (< 2 $cm^2V^{-1}s^{-1}$),[16] poor stability and device-to-device variability. Additionally, the high operating voltage is a disadvantage for portable, battery-powered device applications.[15,16] Moreover, the n-type organic semiconductors have even much lower mobilities (10^{-3} to 10^{-2} $cm^2V^{-1}s^{-1}$), limiting their use in applications such as CMOS.[17]

In this paper, we report the fabrication of high-performance oxide TFTs using p-type SnO_x channel layer deposited by rf magnetron sputtering at room temperature that is post-annealed up to 200ºC. SnO has a specific electronic structure associated with the presence of divalent tin (SnII), in a layered crystal structure.[18,19] SnO has an indirect band structure with major contribution from Sn 5*s* and O 2*p* orbitals near the valence band maximum (VBM) and Sn 5*p* orbitals towards the conduction band minimum (CBM). The origin of p-type conductivity in SnO is mainly attributed to the Sn vacancy and the O interstitial where tin is in Sn^{2+} oxidation state.[18,19] If there is excess oxygen in the film, some cations will be transformed into Sn^{3+} to maintain electrical neutrality. This process is considered as Sn^{2+} capturing a hole and forming weak bonded holes which are located inside the bandgap near the top of the valence band as localized acceptor states.[20,21]

For a set of practical applications, there are a clear demand for p-type TFT able to match the requirements to grow ultra-low power electronics systems, whose key components are based CMOS technology [22]. Apart from that, the emerging flexible electronics, is pushing for processing devices at low process temperatures, together with high mobility and high on-off ratios [7].

TFTs based on p-type SnO_x are expected to fulfill these requirements due to the particular nature of band structure. [20,21] Contributions from Sn 5*s* states to VBM could offer appreciable hole mobility in this material, without using high processes temperature [23,24]. In the present work, SnO_x based TFTs are prepared by an industrial friendly rf magnetron sputtering system at room temperature (RT), without any intentional substrate heating during the growth process, aiming to understand the role of structure, surface finishing and composition in producing high stable TFT with high electronic performances, such as field effect mobility and on-off- current ratios.

2. Materials and Methods

Prior to process the TFT devices, the material in which the channel is based was processed and fully analyzed, concerning their structure, morphology, composition and electro-optical properties, aiming to determine the best conditions to grow the channel layers of the TFT with a bottom gate configuration

Films Preparation

SnO_x films were deposited on glass substrates using a computer controlled rf magnetron sputtering system using a metallic tin target (99.999% pure). Depositions were carried out in a controlled atmosphere of oxygen and argon. Sputtering power to metallic tin target was fixed at 40 W and substrates were rotated at a speed of 40 rpm. Experiments were performed by varying O_{pp} ($O_{pp}=PO_2/(PO_2+PAr)$, where PO_2 and PAr are partial pressures of oxygen and argon) up to 20% in the

deposition chamber, keeping the total deposition pressure constant at 0.2 Pa. At this condition, the deposition rate was 40 Å/min.

Structure and composition studies

X-ray diffraction analysis was performed on tin oxide thin films deposited on glass substrates, using PANalytical X'Pert Pro system, as depicted in Fig.1.

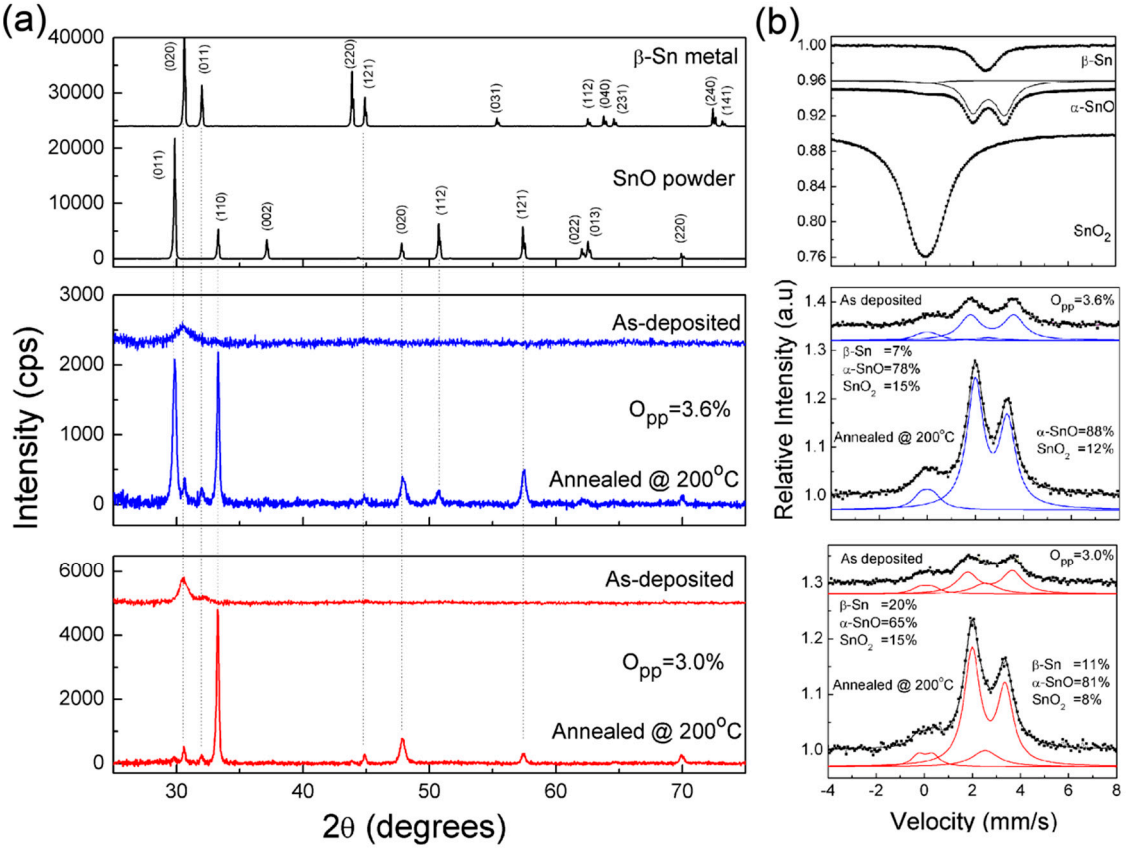

Figure 1: (a) XRD patterns of deposited SnO_x thin films. (b) Transmission ^{119}Sn Mössbauer spectra of bulk samples and CEMS spectra of as-deposited and annealed SnO_x films deposited at 3.0% and 3.6% O_{pp}.

^{119}Sn Mössbauer spectra analysis

The films were analyzed by ^{119}Sn conversion-electron Mössbauer spectroscopy (CEMS) at room temperature placing them inside a proportional backscatter detector RIKON-5 (Wissel) in flowing 5%CH_4-95% He gas mixture (see figure 1b). Both CEMS and transmission Mössbauer spectra were collected using a conventional constant acceleration spectrometer and a 5 mCi $Ca^{119m}SnO_3$ source. The velocity scale was calibrated using a ^{57}Co (Rh) source and an α-Fe foil. The Sn isomer shifts (IS) are given relative to $BaSnO_3$ reference material at 295 K and obtained by adding 0.031 mm/s to the IS relative to the source. The spectra were fitted to Lorentzian lines using a non-linear least-squares method. The set of estimated parameters extracted are depicted in table 1.

Table 1. Estimated parameters from the transmission ^{119}Sn Mössbauer spectra of bulk samples and CEMS spectra of films taken at 295K.

Sample	IS [mm/s]	QS [mm/s]	Γ [mm/s]	Sn phase	I [%]
SnO_2 bulk	0.01	0.56	1.34	-	100
α-SnO bulk	2.67 -0.03	1.34 0.58	0.98 0.77	α-SnO SnO_2	95 5

-Sn metal	2.56	-	1.03	-	100
Film	2.76	1.87	1.04	SnO	65
O_{pp}=3.0%, RT	0.11	0.52	0.84	SnO_2	15
	2.56	-	1.3	-Sn	20
Film	2.7	1.38	0.79	SnO	81
O_{pp}=3.0%,	0.08	0.59	0.7	SnO_2	8
200°C, 30 min	2.56	-	1.35	-Sn	11
Film	2.73	1.82	1.02	SnO	78
O_{pp}=3.6%, RT	0.11	0.53	0.81	SnO_2	15
	2.56	-	1.3	-Sn	7
Film	2.7	1.34	0.82	SnO	88
O_{pp}=3.6%,	0.06	0.48	0.85	SnO_2	12
200°C, 30 min					

IS (mm/s) isomer shift relative to metallic $BaSnO_3$ at 295 K; QS (mm/s) quadrupole splitting; Γ (mm/s) line-width; I relative area. Estimated errors ≤ 0.02 mm/s for IS, QS, Γ and <2% for I.

Electrical studies

It is essential to study the electrical properties of the material in order to understand the charge carrier type and transport properties. Hall Effect measurement is the most commonly used technique to identify the charge carrier and carrier mobility in the material. In contrast to n-type oxides, Hall measurement does not give reliable results for p-type oxides, primarily because of very small drift mobility of holes. Moreover, when both electrons and holes are present in a semiconductor sample, both charge carriers experience a Lorentz force in the same direction. So, both electrons and holes will pile up at the same side of the sample and consequently the measured Hall voltage depends on the relative mobilities and concentrations of holes and electrons. Hall mobility for an ambipolar semiconductor is thus given by,

$$\mu_{Hall} = \frac{n \cdot \mu_n^2 - p \cdot \mu_p^2}{n \cdot \mu_n + p \cdot \mu_p} \quad (1)$$

where n, p, μ_n and μ_p represent electron density, hole density, electron drift mobility and hole drift mobility respectively. This suggests a considerable reduction in Hall mobility in an ambipolar semiconductor compared to the actual drift mobilities of the charge carriers.

In the present analysis, RT deposited samples have shown fluctuations in the sign and magnitude of Hall coefficient. Typical carrier mobilities were of the order of 10^{-1} cm^2 V^{-1} s^{-1}. Because of the ambipolar nature of the RT deposited films [25], these results suggest that Hall measurement of SnO_x films highly underestimates the actual carrier mobility. After annealing up to 200°C for 30 minutes, films prepared in the O_{pp} of 2.8-3.8% have shown positive Hall coefficient consistently. There was no change in Hall coefficient sign even though the magnitudes were shown small fluctuations. This suggests a considerably large density of holes compared to the density of electrons. Figure 2 shows the resistivity variation of as prepared and annealed SnO_x films.

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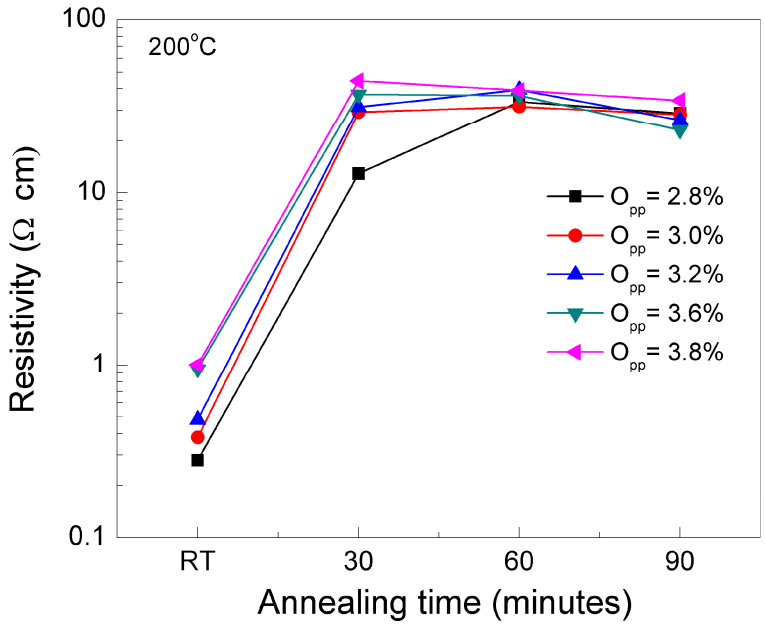

Figure 2: Variation in the resistivity of SnO_x films as a function of annealing time.

As observed in the Mossbauer spectra of RT deposited films, RT samples consist of metallic tin, SnO and SnO_2 phases. In this condition, both electrons and holes can contribute to the charge transport in the system. At 200 °C annealing in air, oxygen atoms incorporate to the films which oxidizes with metallic tin leading to SnO phase formation with reduction in electron density and increase in hole density. This may be the reason for initial increase in the resistivity of the films. In this case, the material has large density of holes compared to the density of electrons which results in positive Hall voltage with typical Hall mobility of 2 $cm^2\ V^{-1}\ s^{-1}$.

Annealing at still higher temperatures cause again a decreasing tendency in material resistivity (not shown here). This time, it is because of the phase transformation of the material from SnO (p-type) to SnO_2 (n-type). Actual carrier mobility must be much higher than the measured hall mobility value.

Optical studies

Optical transmittances of RT deposited films were very poor in the visible region, mainly because of the presence of large concentration of metallic tin in the films (Figure 4a). Annealing up to 200°C for 30 minutes considerably increased the optical transmittance in the visible region. However, still the maximum transmission was around 50%. SnO has been reported as an indirect bandgap material with a direct bandgap value of around 2.5 eV and indirect band gap value around 1 eV. Whereas, SnO_2 is a direct bandgap material with bandgap value around 3.6 eV.

The optical absorption coefficient (α) of semiconductors generally follows a relationship of the form,

$$\alpha \cdot h \cdot \nu = const \cdot (h \cdot \nu - E_g)^r \qquad (2)$$

where $h\nu$ denotes the photon energy, E_g the optical band gap, and r a constant depending on the type of optical transition in the material. The E_g value is then obtained by linearly extrapolating the plot of $(\alpha \cdot h \cdot \nu)^{1/r}$ vs $h \cdot \nu$ and finding the intersection with the abscissa. The optical data in figure 3a

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were analyzed with $r = ½$ (direct transition) and $r = 2$ (Indirect transition). Estimated direct bandgap values are in the range of 2.6 - 2.75 eV for annealed films (figure 3b and 3c). However, the presence of a narrow gap indirect band results considerable optical absorption below these estimated values. The indirect values estimated from a plot of vs results 1.6 - 2.2 eV which is around 1 - 0.55 eV below the corresponding direct bandgap values (figure 3d). These values are close to the reported bandgap values for SnO films. Small variations in these values could be understood on the basis of fractional variations of various phases (metallic tin, SnO and SnO_2) in the films.

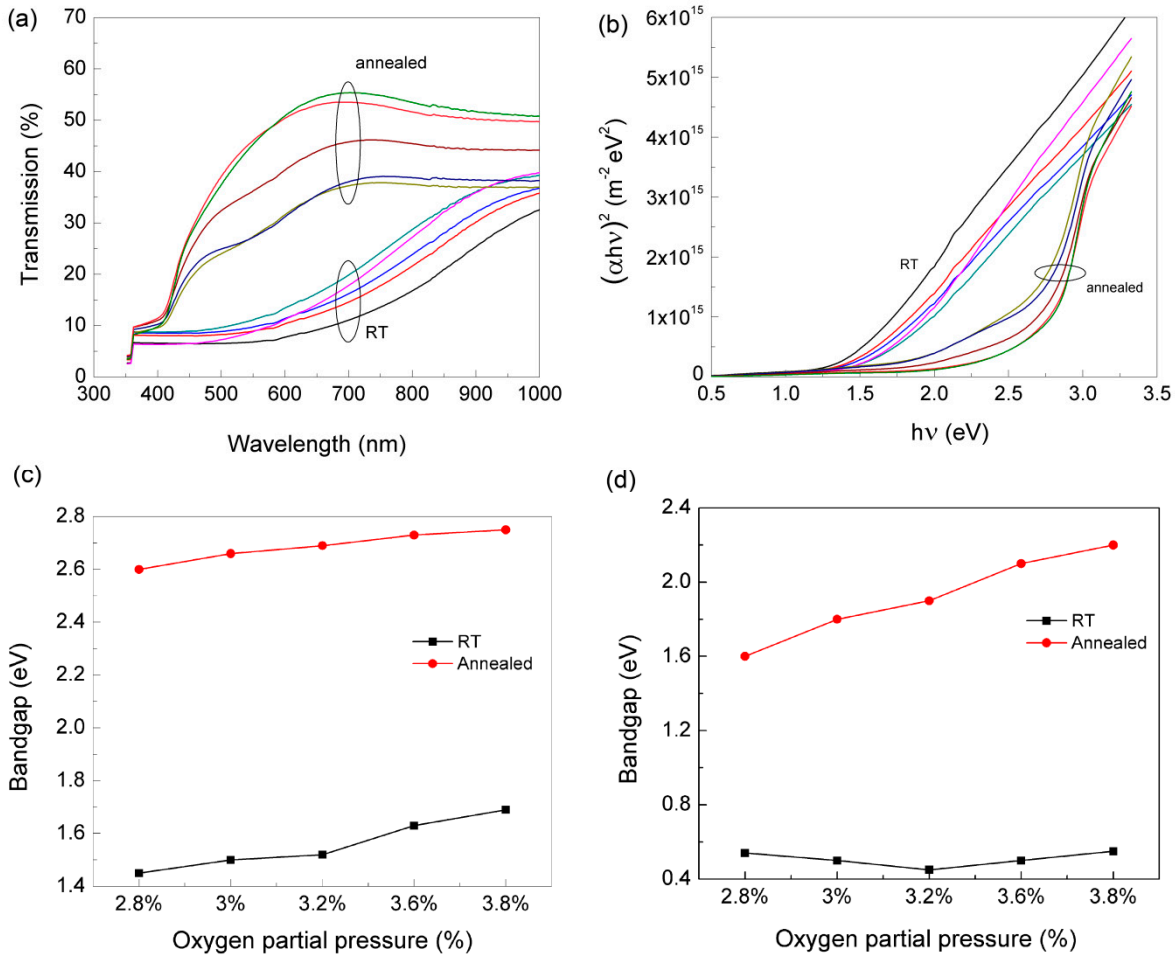

Figure 3: (a) Optical transmission of as prepared and annealed SnO_x films. (b) Plot of vs for direct bandgap estimation. (c) Estimated direct bandgap values and (d) indirect bandgap values.

Devices architecture and structure

Surface morphology of TFT channel layers was analyzed by ZEISS Auriga SEM-FIB and Asylum MFP-3D AFM, as depicted in fig.4.

Bottom gate TFTs were fabricated on glass substrates coated with 150 nm thick layer of sputtered ITO and a 220 nm thick layer of aluminium-titanium oxide (ATO). SnO_x channel layer (width/length=50 m/50 m) was deposited over this by rf magnetron sputtering. Ni/Au (9 nm/60 nm) stacks deposited by electron beam evaporation were used as source and drain electrodes. After deposition, devices were annealed in air up to 200°C for 30 minutes inside a tubular furnace (see figure 4 e).

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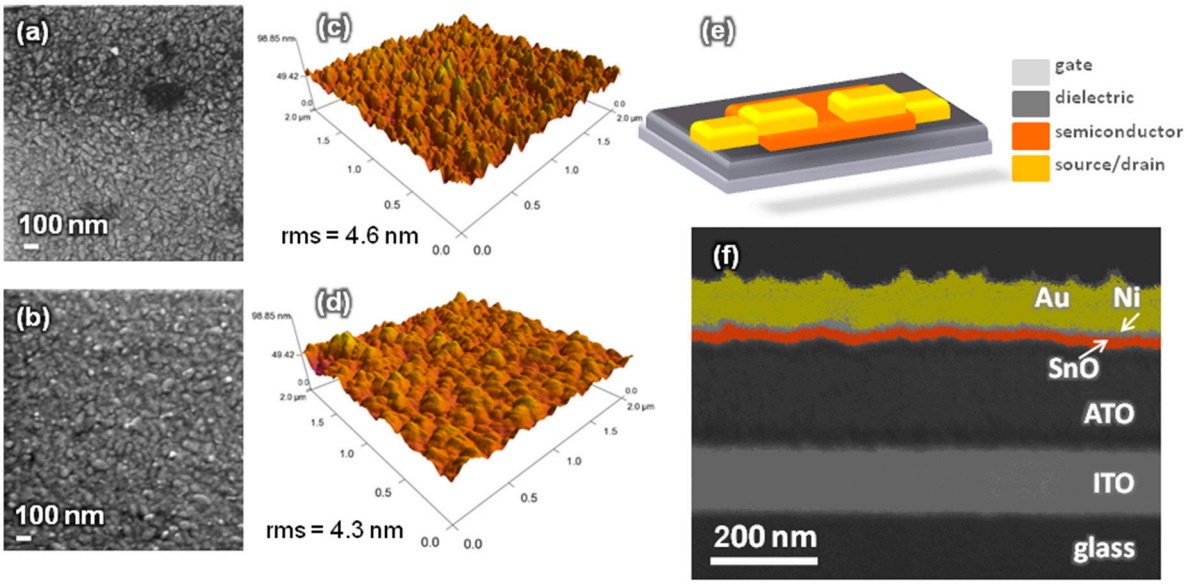

Figure 4. SEM images of post-annealed TFT channel layers prepared at O_{PP} of (a) 3.0% and (b) 3.6%. Corresponding AFM images of the TFT channel layers are shown in (c) and (d). (e) Schematic illustration of SnO_x TFT structure employed for the present study. (f) Cross-sectional SEM image of the SnO_x channel TFT.

TFT electrical characterization was performed with an Agilent 4155C semiconductor parameter analyzer and a Cascade Microtech M150 microprobe station inside a dark box at ambient atmosphere.

Capacitance measurements

CV measurements have been done in TFT by short circuiting the drain and source terminals. By doing so we enhance the overall capacitance measured allowing a better discrimination on the data achieved. Under these conditions, we assume an electrical model consisting in a contact resistance R_C (equal for drain and source regions, since we have a symmetric device) in series with the combination of two parallel RC resonators as depicted in the sketch of figure 5a. One represents the semiconductor channel capacitance (C_S) that varies dynamically, depending on the extension of the accumulation/depletion layer. The other is the interface trap capacitance (C_{it}) in series with the corresponding associated interface resistance R_{it}, both depending on the interface defects given by:

$$C_{it} = \frac{\rho(V)}{dV/dx} = \varepsilon\varepsilon_0 \frac{\rho(V)}{Q} = \frac{q^2 D_{it}}{1+\omega^2\tau_{it}^2} \quad (2)$$

Where D_{it} is the interface trap density, $\tau_{it}=R_{it}\times C_{it}$ is the trap response time. Finally, we have in series the insulator geometric capacitance (C_{ox}). As the frequency tends to steady state condition, we have almost C_{it} in parallel with C_s and the resulting capacitance in series with Cox. Therefore, for not perfect semiconductors (basically, the amorphous ones) by using a frequency modulation less than the relaxation frequency of the semiconductor ($f_r = \frac{1}{2\pi R_B C_s} = \frac{1}{2\pi\rho_B\varepsilon_S\varepsilon_0}$, where R_B is the channel bulk resistance), we expect that capacitance data achieved to be influenced by the number and nature of the interface defects, turning visible more and more defect states as the frequency decreases. The only limit here is the ratios between the screen length and the real thickness of the semiconductor that may

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condition the charge penetration depth. That is, the values of the capacitance can be channel thickness conditioned for devices whose thickness is in the range of few nanometers. On the other hand, at very high frequencies, C_s dominates and $C_{it} \cong 0$, being now relevant the role of R_{it} in parallel with C_{ox}. In this case the capacitance-voltage curves can be distorced due to charging effects, leading to a decrease or even to a not well-defined flat capacitance maximum (C_{max}), as observed in the normalized CV plots of figure S3b for different frequencies and on the behaviour of C_{max} with the frequency, depicted in figure S3c. In the same picture it is also plotted the transfer characteristics of the p-type TFT under analysis (picture above whose vertical scale is on the right side of the figure). Besides the hysteresis that we associate to the role of interface defects, we notice that at a frequency of about 100 Hz the capacitance tends to reach a flat behaviour and the hysteresis voltage shift is enhanced, following a similar trend as the one of the transfer I-V TFT characteristics. We associate this behaviour to interface localized states that only respond at frequencies below f_r as expected.

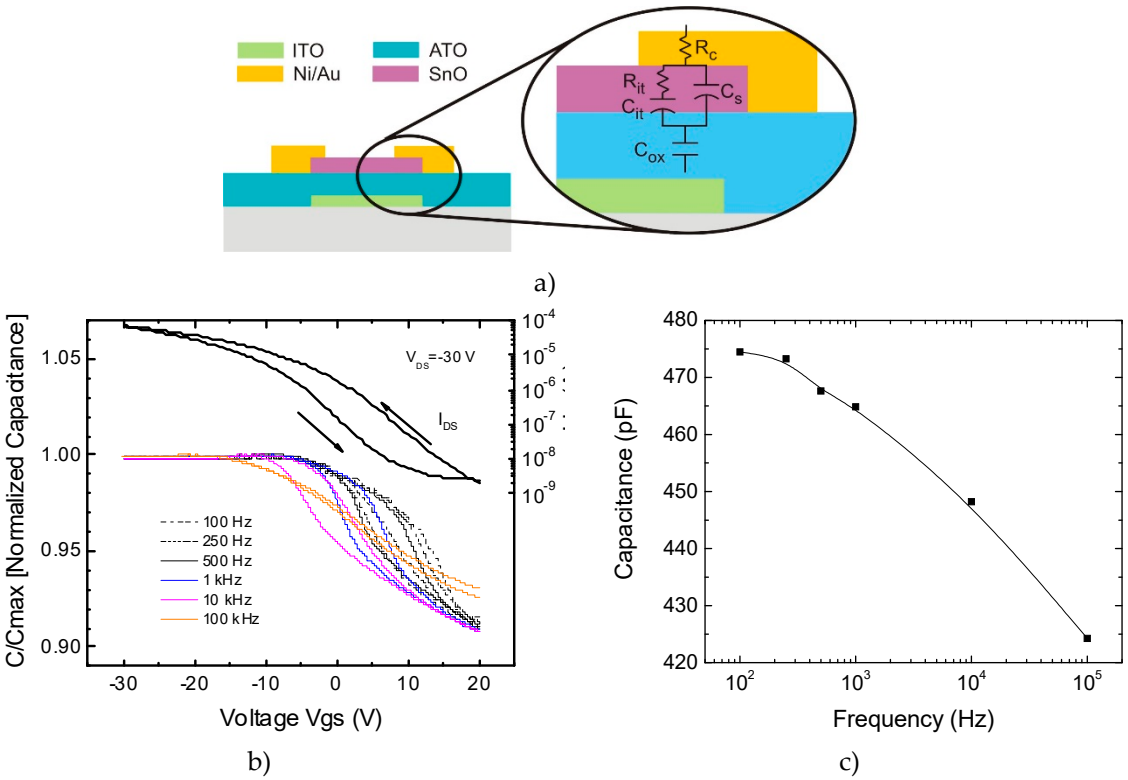
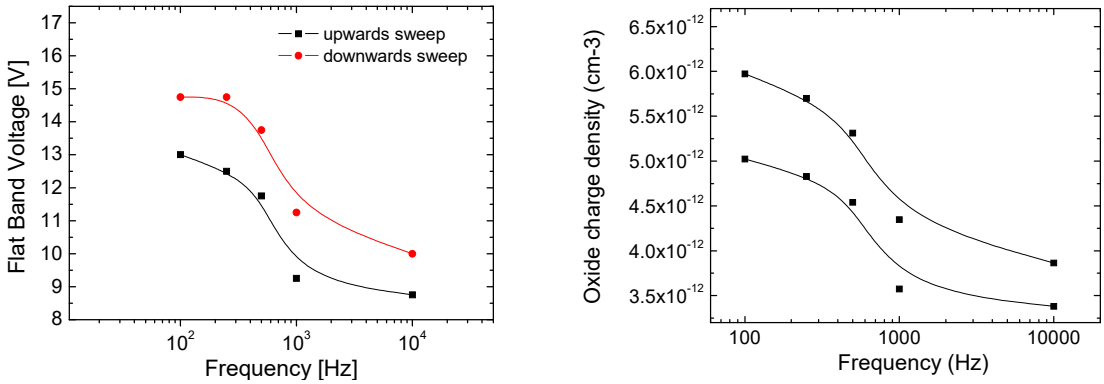


Figure 5. a) Sketch of the cross section of the p-type TFT showing half of the equivalent electrical circuit based on RC resonators b) Normalized CV plot for several frequencies (below), showing also the IV transfer characteristic of the TFT (above); c) The Maximum capacitance (C_{max}) achieved as a function of the frequency used.

Apart from that we notice that the minimum capacitance is not fully flat. This behaviour we associate to the small thickness of the semiconductor (≤ 12 nm) that limits the maximum dimension of the depletion region we can get. As the possible maximum width of depletion region is 12 nm (the semiconductor thickness), this means that the minimum capacitance of the system won't be much lower than the total capacitance.

From the CV plots depicted in Fig. 5 we could also estimate the flat band voltage shift and the oxide charge density (proportional to defect density) as a function of the frequencies used, as depicted in

Fig. 6. There we indicate the two values determined for each frequency due to the hysteresis, defining so the window range of variation of such parameters. For this calculation we assumed a $N_a=10^{17}cm^{-3}$ and a negligible work function difference between the gate electrode and the semiconductor.



a) b)

Figure 6. a) Flat band Voltage dependence on the frequency; b) Oxide charge density as a function of the frequency.

Both plots show a similar dependence on frequency as expected, leading to an enhancement on the flat band voltage and on the oxide charge density as the frequency decreases.

3. Results and Discussion

The SnO_x films were prepared at different oxygen partial pressures (O_{PP}) between 0% and 20%, but the p-type conduction was observed only between 2.8-3.8%. The films deposited with O_{PP} below 2.8% were metallic with poor adhesion to the substrate. Those deposited above 3.8% were highly resistive, showing n-type conduction after annealing above 200 °C. This is well understood based on tin oxide's two well-known forms: SnO (p-type conduction) and SnO_2 (n-type conduction). Since a metallic tin target was used for sputtering, very low O_{PP} was not sufficient to fully oxidize the film. It is believed that O_{PP} in the range of 2.8-3.8% are suitable to form SnO phase and for O_{PP} 3.8% favours SnO2 formation. Since TFTs were prepared for two O_{PP}, namely at 3.0% and 3.6%, most of the materials characterizations were performed using the films deposited at these conditions.

Figure 1 (a) shows the x-ray diffraction (XRD) pattern of the films (120 nm thickness) using Cu Kα line. It shows that RT films have large portion of metallic tin with very small SnO phase. After annealing up to 200°C for 30 minutes in air, part of metallic tin seems to be oxidized to SnO phase. The XRD patterns obtained (in the similar conditions) from SnO powder and metallic Sn are also shown in figure 1.

In order to evaluate the structure, composition of the films and the ratio of SnO and SnO_2 phases present in the TFT channel layer, ^{119}Sn Mössbauer spectroscopic studies were performed for the first time in this type of work, whose results are shown in figure 1 (b). Transmission Mössbauer spectra of bulk metallic Sn, SnO and SnO_2 samples (figure 1b, table 1) were obtained in order to compare the corresponding hyperfine parameters with those of the phases detected in the films by conversion-electron 119Sn Mössbauer spectroscopy (CEMS). The spectra of the bulk samples are identical to those reported in the literature for β-Sn, α-SnO and SnO_2, respectively.[26,27] The α-SnO spectrum shows a small contamination of SnO_2 at lower Doppler velocities, which is a common contamination of α-SnO when exposed to air and is easily detectable by Mössbauer spectroscopy due to the higher recoilless fraction of Sn^{4+} in SnO2 as compared to Sn^{2+} in α-SnO.[28,29] The typical asymmetry of the α-SnO doublet, the high velocity peak having a higher relative area than the low-velocity peak, is also observed.[27-30]

The CEMS spectra of the samples could be fitted by three contributions with typical isomer shifts (IS) of Sn^{4+}, Sn^{2+} and metallic Sn. For all spectra, the estimated IS of the absorption peak due to metallic Sn (table S1) is very similar to that of β-Sn, confirming the presence of this phase in the films as corroborated by XRD. The observed IS, quadrupole splitting (QS) and the line widths of Sn^{2+} in the as-deposited samples are higher than the corresponding parameters for bulk α-SnO. After annealing, the decrease of IS and QS lead to values, which within experimental error, are close to those of crystalline α-SnO. This suggests that the Sn^{2+} oxide present in the as-deposited film is amorphous and after annealing up to 200ºC crystalline α-SnO is formed. This is in agreement with XRD data which shows this phase in the annealed samples while in the as-deposited films only β-Sn is detected. The estimated QS and line widths in the amorphous SnO are higher than in crystalline α-SnO denoting a more asymmetric environment and a higher diversity of near neighbour configurations of Sn^{2+} in the amorphous lattice. Furthermore, no asymmetry is observed for the Sn^{2+} oxide doublet in the as deposited sample as expected for an amorphous phase. As crystalline α-SnO is formed, asymmetry of the corresponding doublet becomes evident.

Mössbauer data, in agreement with XRD data, show that in the as-deposited films most Sn is present as amorphous SnO and metallic β-Sn. Minor amounts of SnO_2, only detected by CEMS, are also present. The IS and QS of this SnO_2 deduced from the spectra are slightly different from those of bulk SnO_2 probably due to poor crystallinity of this oxide in the film. Even though the recoilless factors of β-Sn, SnO and SnO_2 in films are not exactly known, these factors are not expected to be very different for the same species in the different samples. So, the fraction of Sn atoms in each phase should follow the same variation, with annealing or with O_{pp} during deposition, as the relative areas of the corresponding contributions to the spectra. Not surprisingly, the fraction of Sn present as β-Sn is lower in the film deposited at higher O_{pp} (3.6%), than in those deposited at 3.0%. Annealing up to 200ºC not only crystallizes amorphous SnO to form α-SnO but also oxidizes β-Sn to α-SnO. So, it suggests that the TFT channel layer is mainly composed of SnO phase with a smaller contribution from metallic tin and hence we can represent the channel material composition as SnO_x with $1<x<2$.

In order to understand the surface morphology of the channel layer, we performed scanning electron microscopy (SEM) and atomic force microscopy (AFM) of the real channel layer in the TFTs after annealing. The surface microstructures obtained from the films deposited at 3.0% and 3.6% O_{pp} are shown in figure 2. Even though there is no difference in the shape of the grains as evidenced by both techniques, the size of the grains obtained from the films deposited at O_{pp}=3.0% is slightly lower than those deposited at O_{pp}=3.6%. The route mean square roughness (4.6 nm) of the films deposited at Opp=3.0% is slightly higher than that deposited at 3.6% (4.3 nm). Cross-sectional SEM image obtained from the TFT prepared at 3.0% O_{pp} (figure 2f) shows perfect coverage of SnO_x channel layer over the insulator surface with highly compact, uniform and homogeneous thin film without visible defects.

Bottom gate TFTs were fabricated using aforementioned SnO_x films as channel layers (~28 nm thickness) deposited at 3.0% and 3.6% O_{pp}, which were annealed in air up to 200°C for 30 minutes inside a tubular furnace. Despite the high saturation mobility (4.3 $cm^2V^{-1}s^{-1}$) the on-off ratio was very poor (3×10^1) and TFTs operated in depletion mode, which may be due to a large hole density in the channel layer, limiting the channel modulation.

TFT performance was improved by reducing the channel thickness to ~12 nm. The output characteristics (I_{DS}-V_{DS}) of such TFT (O_{pp}=3.0%) given in figure 7a shows excellent p-channel behaviour. The gate voltage was varied from 0 V to -50 V in -10 V steps. Very small I_{DS} at zero gate voltage indicates an almost closed channel. On increasing the gate voltage to higher negative values, holes accumulated at the channel-insulator interface forms a conduction path between source and drain. These TFT exhibits hard saturation at large V_{DS}, which is similar to pinch off in usual field-effect transistors, revealing the high quality of the devices.

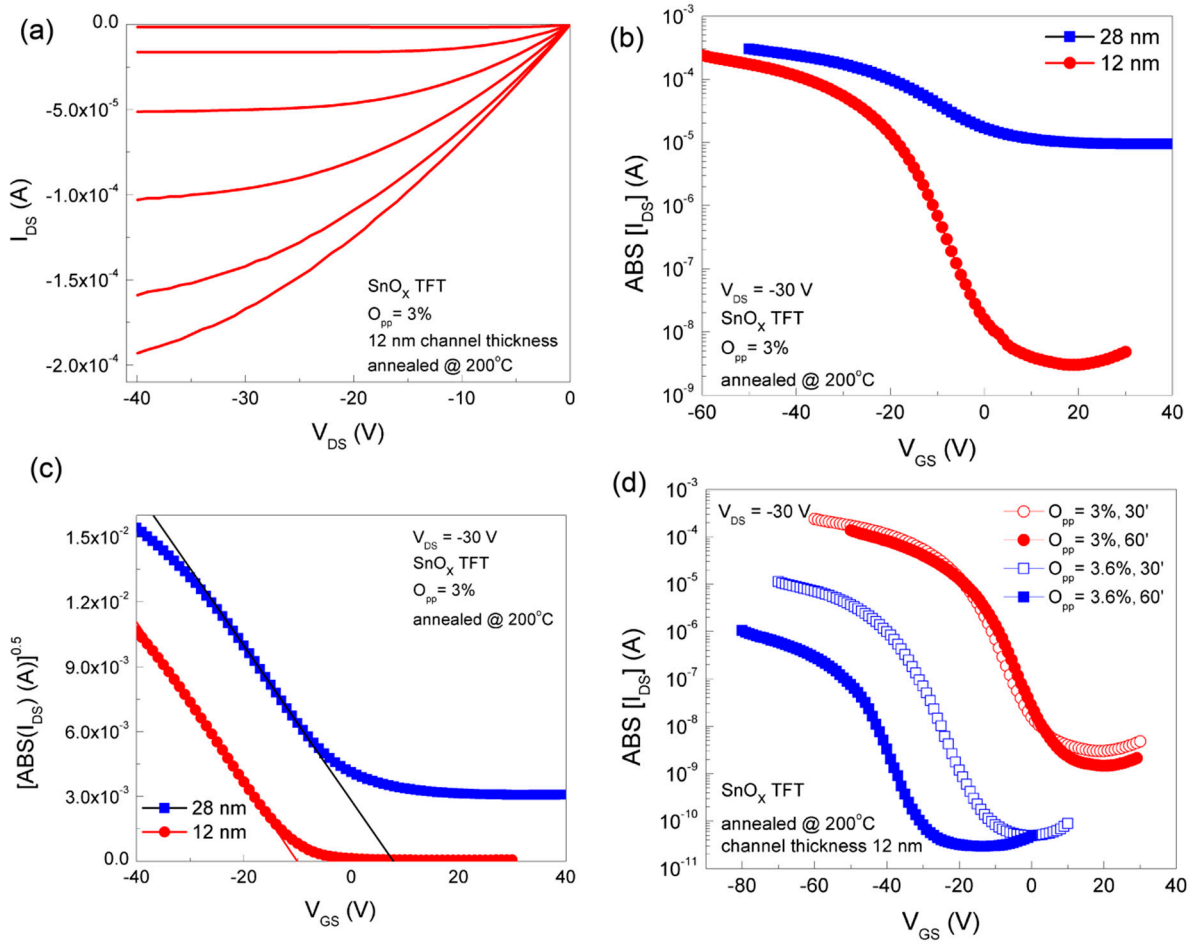


Figure 7. (a) Output characteristics of SnO_x p-channel TFT. The gate voltage is varied from 0 V to -50 V in -10 V steps. (b) Transfer characteristics of SnO_x p-channel TFT with different channel thickness. (c) Plot of square root of drain current, at V_{DS}= -30 V, for evaluating saturation mobility and threshold voltage. (d) Transfer characteristics of SnO_x p-channel TFT (channel thickness 12 nm) for different annealing time.

TFT parameters (see table 2) were extracted from the transfer characteristics ($ABS(I_{DS})$-V_{GS}) of the p-channel TFTs for the different O_{pp} and annealing times used, for devices annealed at 200°C (figures 7 b and 7c). The field effect mobility (μ_{FE}), extracted from the slope of the linear region of the I_{DS}-V_{GS} plot, was 3.3 $cm^2V^{-1}s^{-1}$ for the TFT with 12 nm channel thickness. The saturation mobility (), extracted from $[ABS\ (I_{DS})]^{0.5}$ - V_{GS} plot at V_{DS}= -30 V, was 4.6 $cm^2V^{-1}s^{-1}$ (figure 7c). With the improvement in mobility values, threshold voltage shifted from 8.1 V (28 nm thick channel) to -10 V on reducing the channel thickness to 12 nm. Negative threshold voltage indicates the enhancement mode operation of the p-channel TFTs. Moreover, the off current of the p-type TFTs decreased by several orders by reducing channel thickness which results in good switching action by increasing on-off ratio from ~10^2 to 7×10^4. Figure 7d shows the transfer characteristics of the devices processed at different O_{pp} and for different annealing times. The data depicted show that the best device performances are achieved when using O_{pp} of about 3%, and annealing times of around 30 minutes are more than enough to process devices with excellent stable mobilities and large on-of current rations.

Table 2. Electrical properties of SnO_x p-channel TFTs for different annealing time (channel thickness 12 nm)

Annealing Conditions	Oxygen Partial Pressure [%]	Field Effect Mobility [$cm^2 V^{-1} s^{-1}$]	Saturation Mobility [$cm^2 V^{-1} s^{-1}$]	Threshold Voltage [V]	On-Off ratio
200 °C, 30 min	3.0	3.3	4.6	-10	7×10^4
200 °C, 60 min	3.0	2.2	2.6	-7.2	9×10^4
200 °C, 30 min	3.6	0.16	0.28	-29	2×10^5
200 °C, 60 min	3.6	0.02	0.03	-38.6	3×10^4

The p- channel oxide TFTs fabricated at relatively low temperature in the present work show excellent performance, which can be made even on plastic and paper substrates, surpassing the ones known processed also at low process temperatures, compatible with low cost flexible substrates, such as paper. Moreover, the very high on current of these devices makes them ideal for AMOLED driving circuits where a TFT must supply sufficient hole current to the anode of the OLED. In addition, these SnO_x TFTs show excellent electrical stability even without any passivation layer.

Figure 8 shows the transfer curves of TFTs measured at different days after their fabrication. It is clear from the figure that, these TFTs are very stable in operation without significant variations in threshold voltage and mobility.

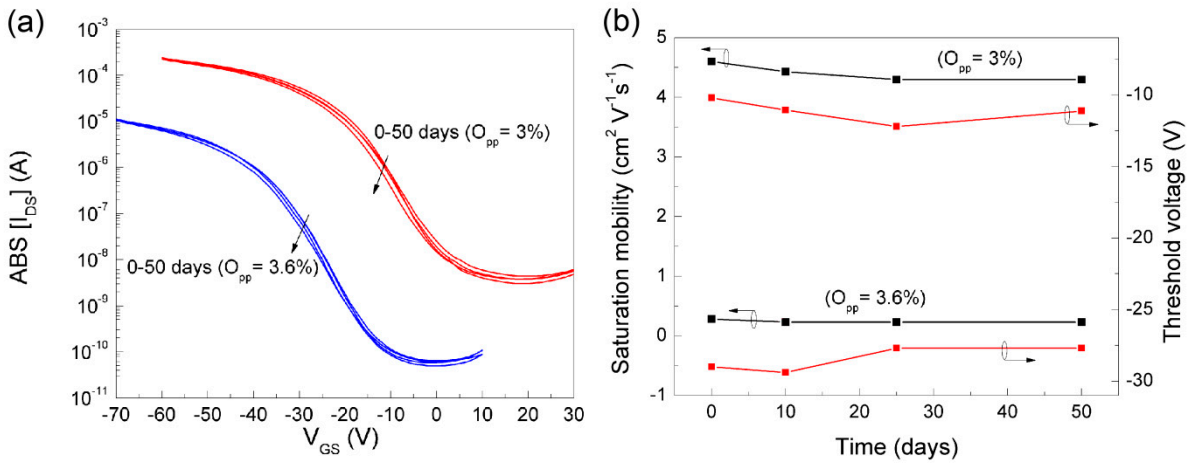


Figure 8. Transfer characteristics of SnO_x p-channel TFT measured at different days after device fabrication (a) and corresponding variations in saturation mobility and threshold voltage (b).

4. Conclusions

In summary, we have fabricated high performance p-channel oxide TFTs (highly reproducible) on glass substrates using SnO_x channel layer, for which the proper process conditions that lead to the best material phase composition were selected. The SnO phase was identified and quantified by the first time by two independent techniques, XRD and Mossbauer spectroscopy, corroborating the p-type oxide semiconductor behaviour obtained in the TFTs. The TFTs fabricated in this work have shown typical saturation mobility of 4.6 $cm^2V^{-1}s^{-1}$ and on-off ratio above 7×10^4, which are the highest values achieved so far from any p-channel oxide TFTs. This breakthrough will enable the production

of fully transparent CMOS associated with all the main advantages offered by transparent/oxide electronics.

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