*Article*

# Current Mode Control of a Series LC Converter supporting Constant-Current Constant-Voltage (CCCV)

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**Abstract:** This paper presents a control algorithm for soft-switching series LC converters. The conventional voltage-to-voltage controller is split into a master and a slave controller. The master controller implements constant-current-constant-voltage (CCCV) control, required for demanding applications, i.e. lithium battery charging or laboratory power supplies. It defines the set-current for the open-loop current slave controller, which generates the PWM parameters. The power supply achieves fast large-signal responses, e.g. from 5 V to 24 V, where 95% of the target value is reached in less than 400 µs. The design is evaluated extensively in simulation and on a prototype. A consensus between simulation and measurement is achieved.

**Keywords:** control; current mode control; voltage control; transfer function; power converter; soft-switching converter; battery charging;

## 1. Introduction

By the use of soft-switching converters high efficiency DC/DC converters can be built. One possible topology, a series LC (SLC) converter is shown in Figure 1. The topology is similar to a series resonant converter, but it operates in a non-resonant push-pull mode [1]. In contrast to a dual active half bridge converter, the two secondary side active output switches are replaced with diodes [2].

A detailed time domain analysis for calculating the SLC output current, operated above the LC resonance frequency was published recently [1]. Current literature proposes a voltage-to-voltage transfer function [3]. We split the voltage-to-voltage converter in a cascaded structure [5]. A master controller sets the SLC output current, while a slave open-loop transfer function controls the switching period, duty cycle and pulse-skipping. The master voltage controller supports constant-current-constant-voltage (CCCV) operation, that is required e.g. for battery charging [6] or laboratory power supplies.

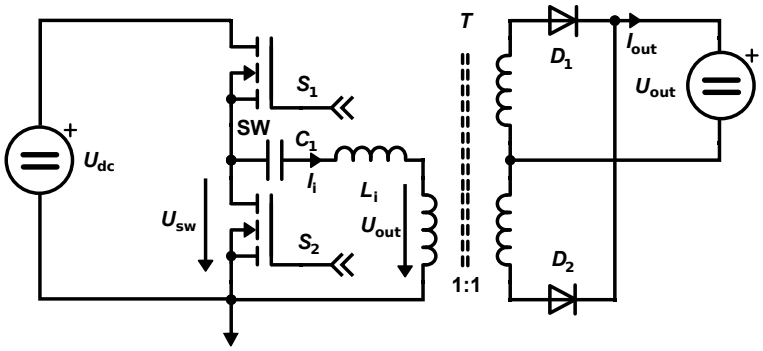


**Figure 1.** The schematic of the series LC converter is identical to the series resonant converter, however the resonant capacitor $C_1$ is chosen large and acts as a DC blocking capacitor. The converter is operated far above its resonance frequency.

Equation (1) formulates the SLC converter output current $I_{cc}$ as a function of the input voltage $U_{dc}$ and output voltage $U_{out}$ based on the control parameters duty cycle $D$ and switching period $t_p$ [1]. By adding pulse skipping, where $p_o$ and $p_c$ represent the pulse skipping parameter defined in Figure 6, a very large output current range can be achieved.

$$I_{cc} = \frac{p_o}{p_c} \frac{D(1-D)U_{dc}^2 - U_{out}^2}{4L_i U_{dc}} t_p \tag{1}$$

As the input voltage and also the output voltage are monitored in (1), this equation allows a very high rejection ratio [1]. The output voltage is $U_{out}$ and the measured output voltage is referred as $U_{meas}$. As large input voltage ripple can be rejected, this allows for a reduction of the DC link capacitance $C_{dc}$. This enables the use of film capacitors instead of electrolytic capacitors, extending the estimated service-life of the power supply.

The proposed control diagram is shown in Figure 2. The control is based on four elements: {1}, the master voltage controller sets the current to the slave current controller. {2}, the slave current mode controller is an open-loop control transfer function, based on (1). The current controller sets four parameters to the PWM modulator {3}. The PWM modulator generates the PWM output waveform for the series LC converter {4}.

The controller is implemented on a digital signal processor (DSP), as (1) requires non-linear calculations. ADCs digitize the input voltage, output voltage and output current for the CCCV control. An MCU with integrated PWM module generates the switching signals for the half bridge.

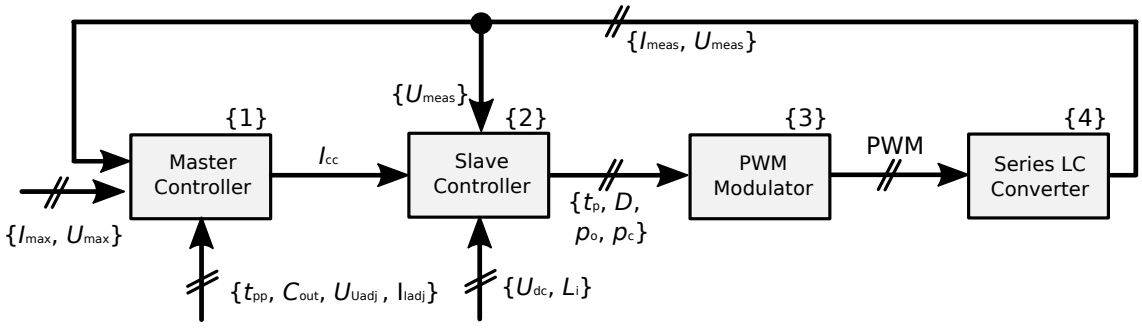


**Figure 2.** Proposed control diagram for the series LC converter. The converter is split into a master controller, implementing CCCV control, and an open-loop slave controller.

## 2. Master Voltage Mode Controller

The master voltage mode controller, is shown in detail in Figure 3. It consists of two controllers: One to control the voltage and one to control the current. Both operate in parallel and the minimum value is selected to control the set current for the constant current controller, $I_{cc}$.

The sensed current $I_{\text{sense}}$ should be filtered to prevent systems oscillation when a capacitive load is connected. In this design, a second order low pass filter with a cutoff frequency of 16 kHz is used. Both controllers are discussed in detail in the following subsections.

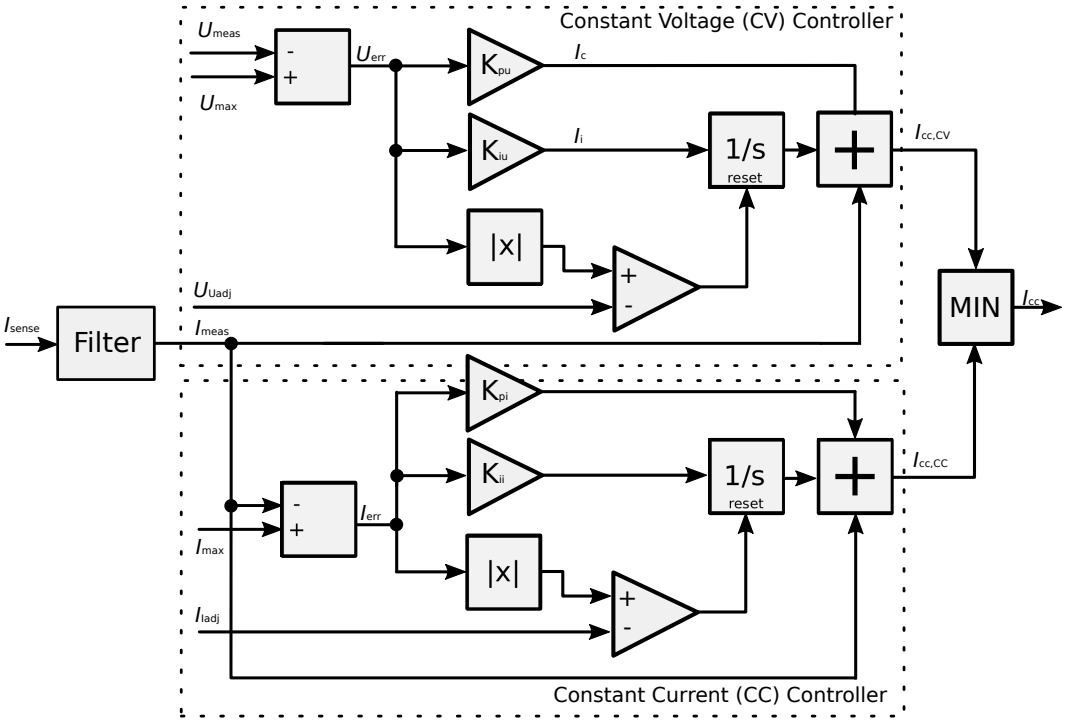


**Figure 3.** The master controller implements the CCCV functionality. The current and the voltage controllers operate in parallel and the smaller set value is selected for the output set current $I_{\text{cc}}$.

### *2.1. Constant Voltage Controller*

The constant voltage controller limits the maximal output voltage to $U_{\text{max}}$. We design the voltage control loop in Figure 3 based on circuit analysis of the output capacitor $C_{\text{out}}$: The required set current $I_{\text{cc,CV}}$ is expressed in (2). The filtered current is designated $I_{\text{meas}}$.

$$I_{\text{cc,CV}} = I_{\text{meas}} + I_{\text{c}} + I_{\text{i}} \tag{2}$$

The equalization current $(I_{\text{c}} + I_{\text{i}})$ is calculated by a PI regulator. The proportional gain is chosen on the charge balance observation: We calculate the proportional equalizing current $I_{\text{c}}$ as a function of the output charge.

$$Q = I_{\text{c}} \cdot t_{\text{pp}} = C_{\text{out}}(U_{\text{max}} - U_{\text{meas}}) \tag{3}$$

$$I_{\text{c}} = \frac{C_{\text{out}}(U_{\text{max}} - U_{\text{meas}})}{t_{\text{pp}}} \tag{4}$$

The time constant $t_{\text{pp}}$ in (5) is chosen according to the maximal digital regulator control loop period. Stability was observed by using a factor of 1/4 or less at a control loop frequency of 85.750 kHz. Hence the P regulator's gain can be formulated as:

$$K_{\text{pu}} \leq \frac{C_{\text{out}}}{4 \cdot t_{\text{pp}}} \tag{5}$$

The DC voltage accuracy is enhanced by increasing the proportional gain $K_{\text{pu}}$. Referring to (5), the output capacitance is proportional to the maximal proportional gain.

An I regulator with reset is used to achieve stationary accuracy of the control. It adjusts a typically small error. To reduce overshoot, it is only activated if the error is lower than an absolute minimal error. We name this minimal voltage $U_{\mathrm{Uadj}}$.

### 2.2. Constant Current Controller

The constant current controller limits the output current to $I_{\mathrm{max}}$. Previous research already demonstrated that the slave output current accuracy $I_{\mathrm{cc}}$ is better than 7% [1]. Therefore, the output current is directly forwarded to the limiter. To compensate for inaccuracies, an additional PI regulator is used. If the absolute error is larger than $I_{\mathrm{Iadj}}$, the I regulator is reset to reduce overshoot for large signal responses.

### 2.3. Acoustic Noise

When multi layer ceramic capacitors (MLCC) are used as output capacitors, they may emit acoustic noise due to the capacitors piezoelectric dielectric. If the master's P gain is chosen close to the critical gain, noise is emitted. The acoustic noise is reduced by lowering the P gain or choosing low noise MLCCs.

Our experiments concluded that the following control loop gain eliminated the noise at the cost of a slightly slower step response.

$$K_{\mathrm{pu}} \leq \frac{C_{\mathrm{out}}}{9 \cdot t_{\mathrm{pp}}} \tag{6}$$

## 3. Slave Current Controller

The slave current controller receives the set current $I_{\mathrm{cc}}$ from the master controller. It is responsible for selecting the appropriate modulation scheme: It chooses between adjusting the switching period, duty cycle or pulse skipping, as shown in Figure 4.

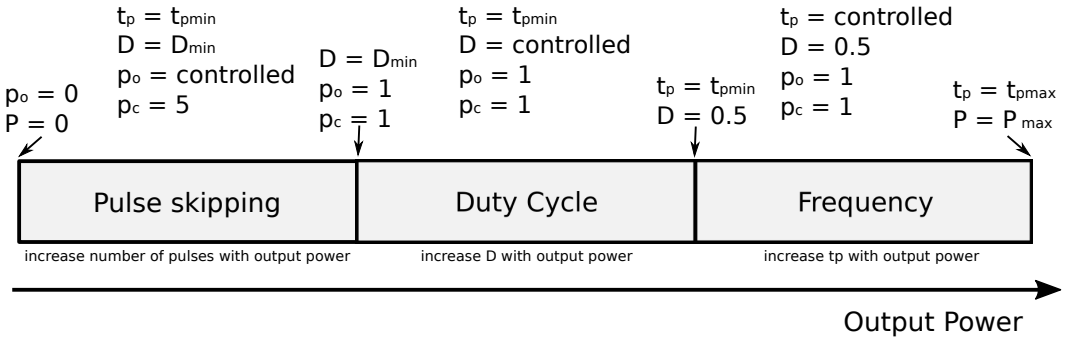


**Figure 4.** The slave current mode controller controls the frequency ($f_{\mathrm{p}} = 1/t_{\mathrm{p}}$) for high output power, the duty cycle ($D$) for medium output power and pulse skipping ($p_{\mathrm{o}}/p_{\mathrm{c}}$) for low output power. This modulation scheme maximises the output current range.

For adjusting the output power we propose the modulation strategy shown in Figure 4. Pulse skipping is used for the lowest possible output power. The number of pulses may range between zero and $p_{\mathrm{c}}$. At medium output power, the duty cycle is increased from $D = D_{\mathrm{min}}$ to $D = 0.5$. At very high output power, the switching period is increased until the maximal allowed $t_{\mathrm{pmax}}$ is reached.

The implementation of the algorithm proposed in Figure 4 is visualized in Figure 5 and is next discussed in detail.

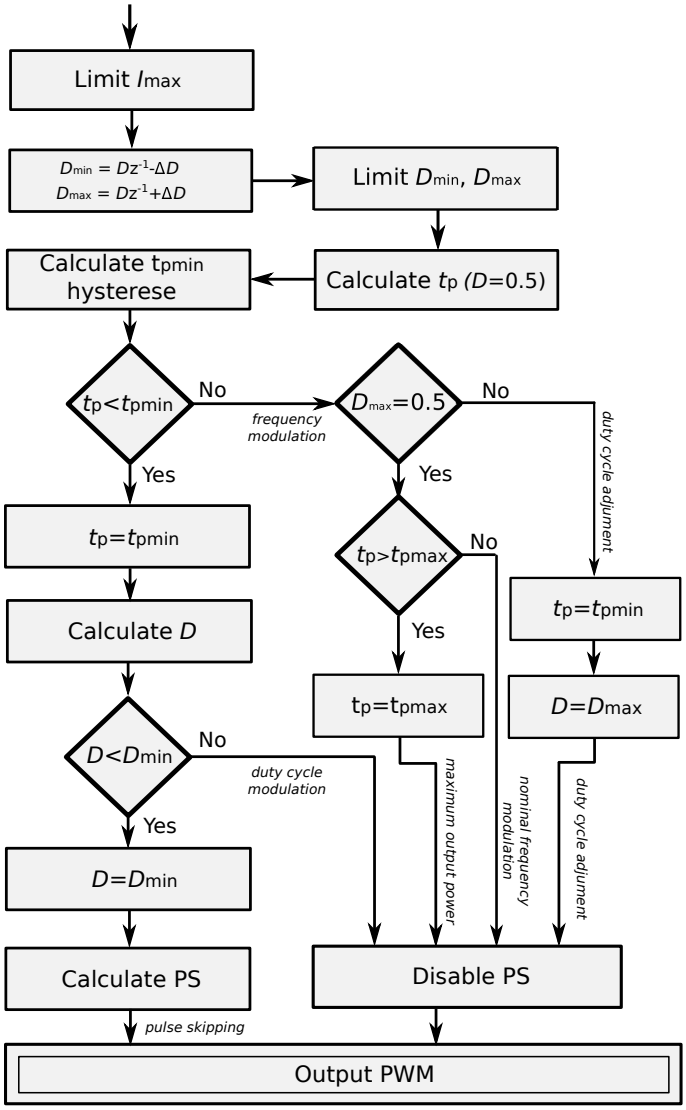


**Figure 5.** Slave current mode controller algorithm

### *3.1. Initial Calculus*

First, the minimal and maximal duty cycle are calculated, which are next limited. Second, the period $t_p$ is determined using (7), which is based on (1), using a duty cycle $D = 0.5$. Next, the minimum period $t_{pmin}$ is calculated, which is a constant value, with an additional hysteresis. In the simulation and experiments, no hysteresis was utilized. The maximum switching frequency is typically chosen in such a manner, that soft-switching of the half bridge can still be achieved.

$$t_p = \frac{16 L_i U_{dc} I_{cc}}{U_{dc}^2 - 4 U_{meas}^2} \tag{7}$$

### *3.2. Frequency Modulation*

If the period $t_p$ is larger than $t_{pmin}$, switching frequency modulation is used. To prevent the unintentional false-triggering due to displacement current, the minimal period $t_{pmin}$ is used during duty cycle adjustment. A duty cycle adjustment is in progress, when $D_{max} < 0.5$.

### 3.3. Duty Cycle Modulation

If the period $t_\mathrm{p}$ is smaller than $t_\mathrm{pmin}$, the duty cycle modulation is used. The duty cycle can be determined by (1). As a quadratic equation has two results, one has to be chosen. To limit the voltage stress on $C_1$, the smaller resulting duty cycle is used. This results to the following equation:

$$D = \frac{U_\mathrm{dc}\, t_\mathrm{pmin} - \sqrt{(U_\mathrm{dc}^2 - 4U_\mathrm{meas}^2)\; t_\mathrm{pmin}^2 - 16 I_\mathrm{cc}\, L_\mathrm{i}\, U_\mathrm{dc}\, t_\mathrm{pmin}}}{2 U_\mathrm{dc}\, t_\mathrm{pmin}} \tag{8}$$

### 3.4. Pulse Skipping

If the calculated duty cycle is smaller than the minimum duty cycle $D_\mathrm{min}$, pulse skipping is used. The pulse modulation is calculated according to the following formula, which can be converted to the on-pulse ($p_\mathrm{o}$) and total number of periods ($p_\mathrm{c}$). An example for an PWM waveform with pulse skipping is given in Figure 6.

$$I_{cc} = \frac{p_\mathrm{o}}{p_\mathrm{c}} \frac{D_\mathrm{min}(1 - D_\mathrm{min}) U_\mathrm{dc}^2 - U_\mathrm{meas}^2}{4 L_\mathrm{i} U_\mathrm{dc}} t_p \tag{9}$$

Currently, a fixed pulse skipping period $p_\mathrm{c}$ is used. However, also the Farey method could be used to determine a more accurate ratio [4]. If $p_\mathrm{o} < 0.5$, the PWM output is disabled. Thereby very low pulse counts can be achieved.

### 3.5. Voltage Stress on $C_1$

The voltage $U_\mathrm{c}$ on the offset capacitor $C_1$ can be calculated using the following equation [1]:

$$U_\mathrm{c} = D U_\mathrm{dc} \tag{10}$$

To limit the voltage slope stress on the offset capacitor $C_1$ and slow down its aging, the duty cycle is only changed slowly. Currently a value of $\Delta D = 0.02$ per iteration is used to limit the stress on the DC blocking capacitor $C_1$.

## 4. Modulator

The modulator generates the PWM waveform. It has four input parameters: The period $t_p$, the duty cycle D, the number of emitted pulses $p_\mathrm{o}$, and the number of pulses per period $p_\mathrm{c}$. An example is depicted in Figure 6. The period $t_\mathrm{p} = \frac{1}{f_\mathrm{sw}}$ is the inverse of the switching frequency, and the duty cycle states the ratio of the PWM high period. A switching cycle can be skipped by pulse skipping. The pulse skipping ontime $p_\mathrm{o}$ states how many PWM pulses are emitted during a pulse skipping period $p_\mathrm{c}$.

To prevent acoustic noise by pulse skipping, the pulse skipping frequency, should be larger than the maximal audible frequency $f_a = 20\,\mathrm{kHz}$:

$$\frac{1}{p_\mathrm{c}\; t_{pmin}} > f_a \tag{11}$$

## 5. Simulation and Experimental Results

The following section covers the simulation and measurement results for the CCCV converter.

### 5.1. Measurement Setup

To verify operation, the circuit is simulated with the software PLECS and tested in an experimental setup. The build converter prototype is shown in Figure 7. The test parameters are shown in Table 1, unless otherwise noted. For the simulations and experiments, a load resistor of $R_\mathrm{load} = 10\,\Omega$ is connected to the output.

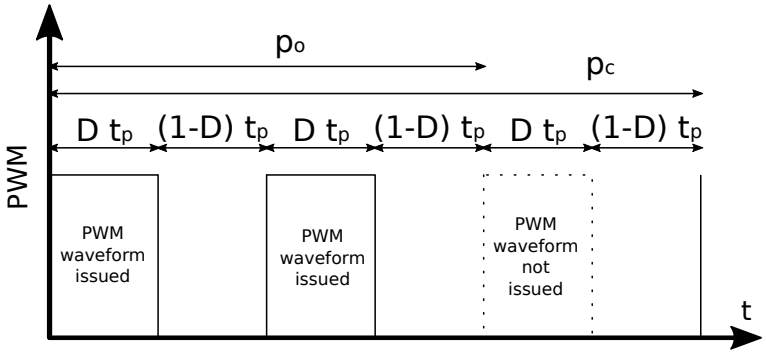


**Figure 6.** A PWM pulse skipping waveform is shown, where the period ($t_p$), duty cycle ($D$), and pulse skipping ontime ($p_o = 2$) and pulse skipping period ($p_c = 3$) are highlighted.

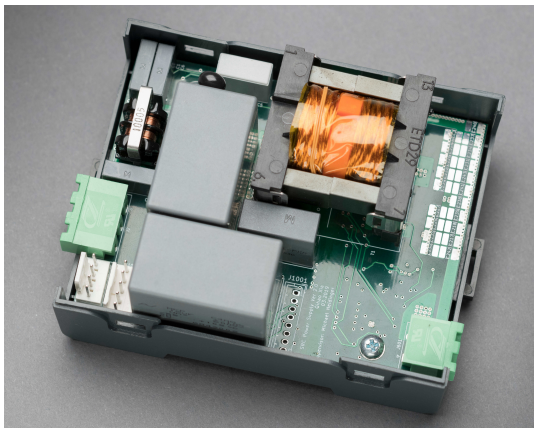

**Figure 7.** The prototype is mounted in a DIN rail case. It avoids electrolytic capacitors, and replaces them with film capacitors to achieve a longer service life.

Four tests are carried-out: {1}, a constant voltage step response test, {2} a constant current step response test, {3} a load response test and in {4}, the CCCV step response is verified. For each test setup, the corresponding output current and voltage are measured in the prototype. Additionally for each test pattern, output voltage and current are simulated as well. The depicted duty cycle and switching period are extracted from simulation only.

**Table 1.** Test setup parameters and conditions

| Element/Parameter | Value |
|---|---|
| $U_{\text{in}}$ | 325 V |
| $T_{\text{ratio}}$ | 4.2:1 |
| $L_{\text{i}}$ | 110 µH |
| $C_1$ | 470 nF |
| $C_{\text{out}}$ | 110 µF |
| $K_{\text{pu}}$ | 1.0 |
| $K_{\text{iu}}$ | 857.5 |
| $U_{\text{Uadj}}$ | 0.05 $U_{set}$ |
| $K_{\text{pi}}$ | 20 |
| $K_{\text{ii}}$ | 17150 |
| $I_{\text{Iadj}}$ | 0.05 $I_{set}$ |
| $\Delta D$ | 0.02 |
| $D_{\text{min,abs}}$ | 0.2 |
| $t_{\text{pmin}}$ | 5 µs |
| $p_{\text{c}}$ | 5 |
| $f_{\text{control}}$ | 85.750 kHz |

### 5.2. Voltage Step Response

The constant voltage controller limits the allowable output voltage. To verify the constant voltage controller, the maximal output voltage $U_{max}$ is increased in a step response at $t = 0$ from 5 V to 24 V and the step response is shown in Figure 8.

Before the step, $t < 0$, the duty cycle $D$ is limited at $D_{min} = 0.2$. When the output power increases after $t = 0$, the duty cycle $D$ increases each control loop iteration by steps of $\Delta D = 0.02$ to $D = 0.5$ for achieving maximum output power. After the duty cycle ramp-up, at $t \approx 180\,\mu s$, the switching period is limited to ensure over-resonant operation. When the set output voltage $U_{meas}$ is about to reach the maximal voltage $U_{max}$, the switching frequency is reduced.

In Figure 8, the output voltage rises fast and reaches 95% of the target output voltage in less than 400 µs. A transition from pulse skipping at low load to switching frequency modulation at high load is demonstrated.

When the measured output voltage from the experiment $U_{meas}$ is compared to the simulated output voltage $U_{sim}$ in Figure 8, a consensus is observed. The non-congruence between $t \approx 300\,\mu s$ and $t \approx 600\,\mu s$ arises due to non-linear MLCC capacitance.

### 5.3. Current Step Response

The constant current controller limits the maximum allowable output current. For the verification, the maximal output current $I_{max}$ is increased from 1 A to 2 A. The output current step response is shown in Figure 9. Before $t = 0$, the converter operates in pulse skipping mode. Pulse skipping generates a significant ripple on the output voltage, as the effective switching frequency is very low.

At $t = 0$, the output current $I_{max}$ is increased from 1 A to 2 A, and the duty cycle is increased from $D = 0.2$ to $D = 0.5$ in increments of $\Delta D = 0.02$, while using the minimal period $t_p$ to prevent over-current triggering. For charging the output capacitor $C_{out}$ the slave controller first utilizes frequency modulation, but switches at $t \approx 230\,\mu s$ back to duty cycle modulation because the amount of required output power is reduced.

Current control reaches 95% of the output current target in $t \approx 300\,\mu s$. At $t < 400\,\mu s$ the fine adjustment by the PI regulator is complete. The converter did not overshoot on the output current.

When the measured output current from the experiment $I_{meas}$ is compared to the simulated output current $I_{sim}$ in Figure 9, a consensus can be observed. The slight difference is due to the non-linear MLCC capacitance.

### 5.4. Load Response

The load response monitors the output voltage change while the load is increased. For this experiment, shown in Figure 10, the output voltage is held constant at $U_{max} = 5\,V$ while an external current load is increased from $I_{meas} = 0.5\,A$ to $I_{meas} = 2\,A$ at $t = 0$ . The output capacitor was chosen in this experiment to $C_{out} = 150\,\mu F$.

Before $t < 0$, the converter operates in pulse skipping mode, explaining significant output ripple. At $t > 0$ the output current $I_{out}$ increases to 4 A. The duty cycle is increased by $\Delta D = 0.02$ to $D = 0.5$. Because of that, the converter cannot supply sufficient output power, hence the output voltage decreases. When the duty cycle adjustment is completed, at $t \approx 170\,\mu s$ the duty cycle is constant at $D = 0.5$, then the switching period $t_p$ instantly increases. An overshoot of $U_{os} \approx 0.1\,V$ is observed in simulation. However, in the experiment this overshoot could not be measured. It must be denoted that the presented load jump represents the worst case.

The load response may be improved by not using the minimal switching frequency during duty cycle adjustment. However, in that case the overcurrent detection level has to be increased.

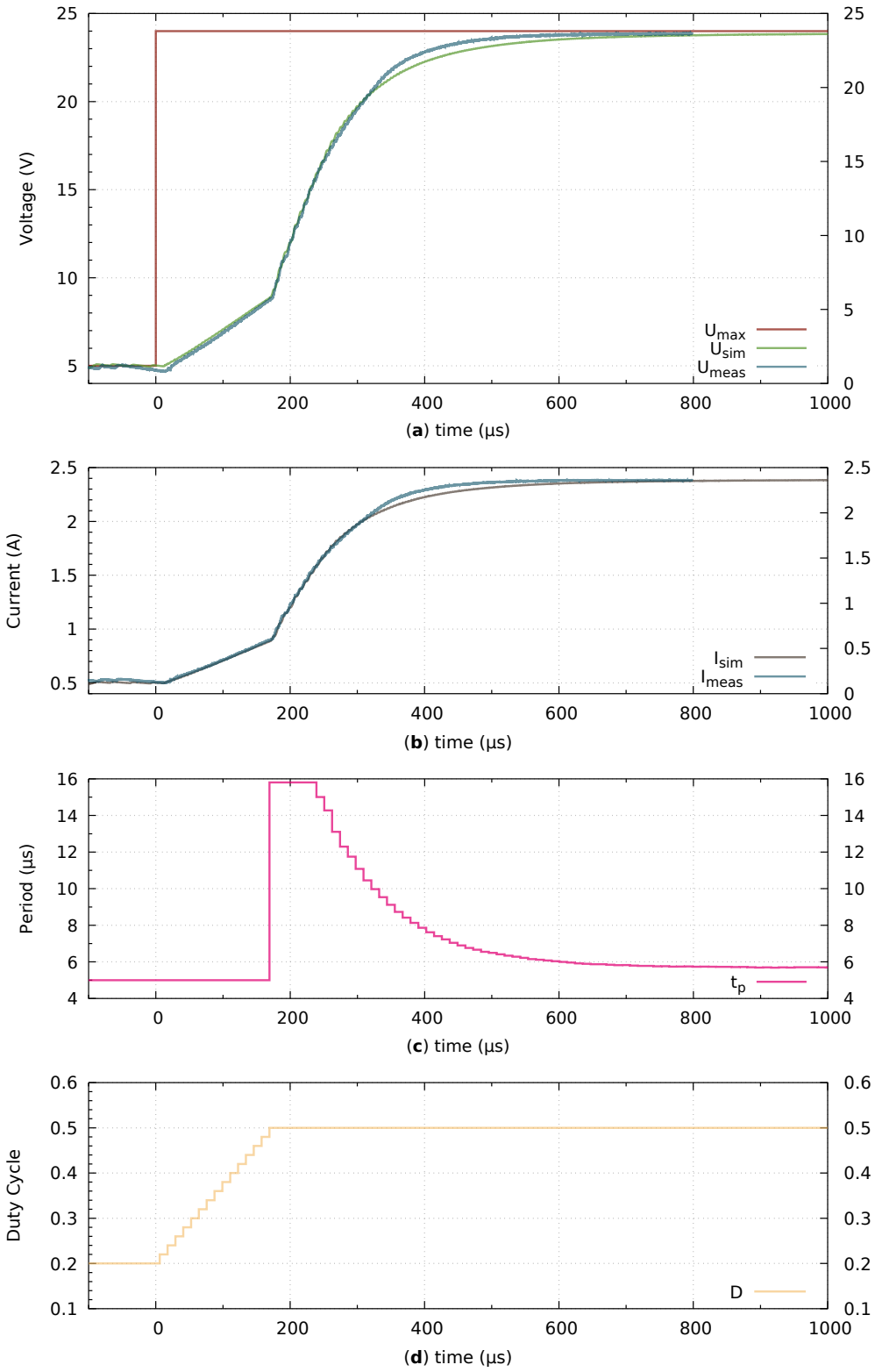


**Figure 8.** The constant voltage operation of the control is verified: The output voltage limit $U_{\max}$ is increased in a step response from 5 V to 24 V (**a**) at $t = 0$ . The simulated and measured output voltage are shown in (**a**). The simulated and measured output current are shown in (**b**). The simulated switching frequency $t_p$ is shown in (**c**), while the simulated duty cycle $D$ is shown in (**d**).

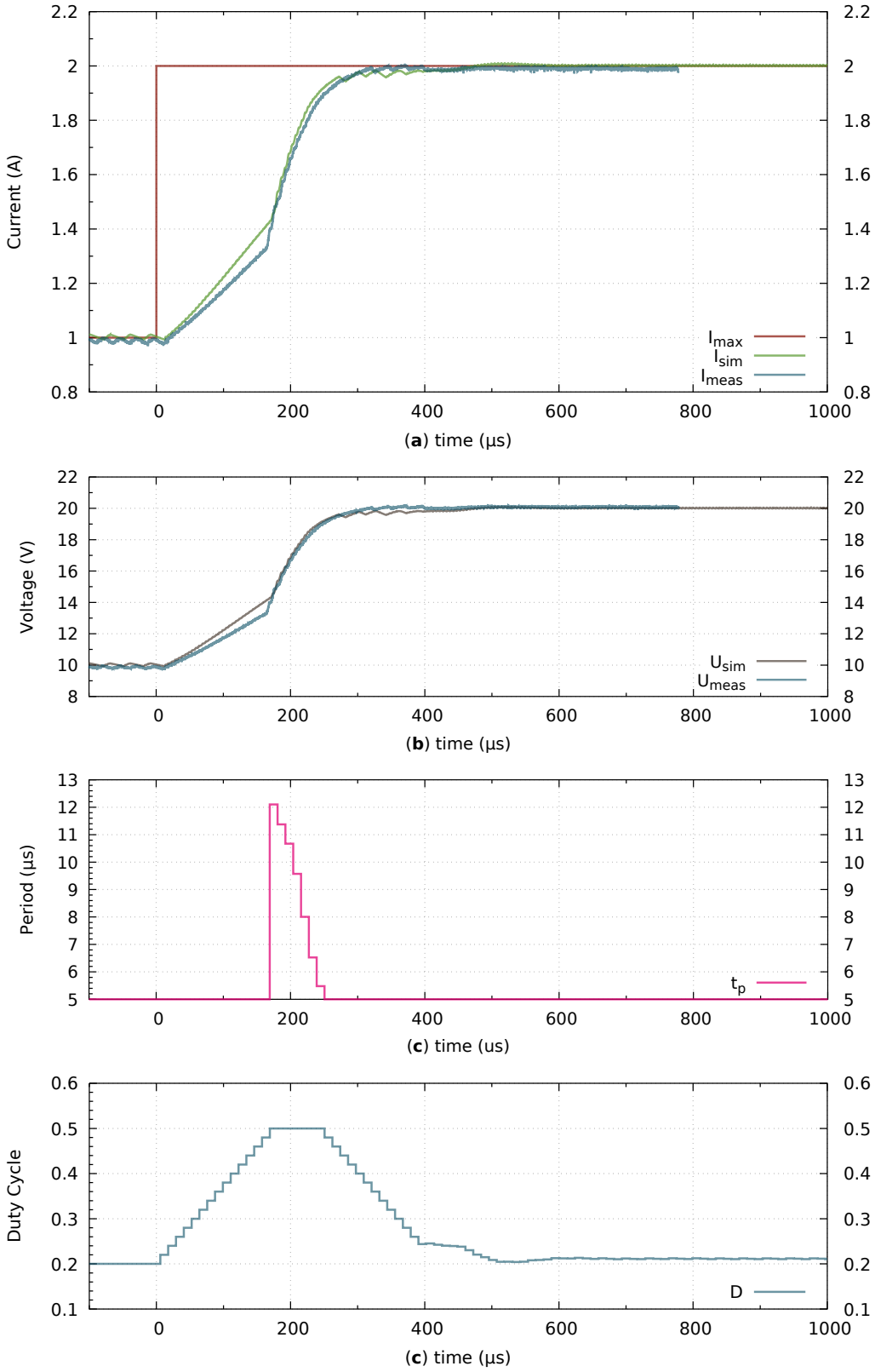


**Figure 9.** The constant current operation of the control is verified: The maximum output current $I_{\max}$ is increased in a step response from 1 A to 2 A (**a**) at $t = 0$. The simulated and measured output current is shown also in (**a**). The simulated and measured output voltage is shown in (**b**), while the simulated switching frequency $t_p$ is shown in (**c**), and the simulated duty cycle is shown in (**d**).

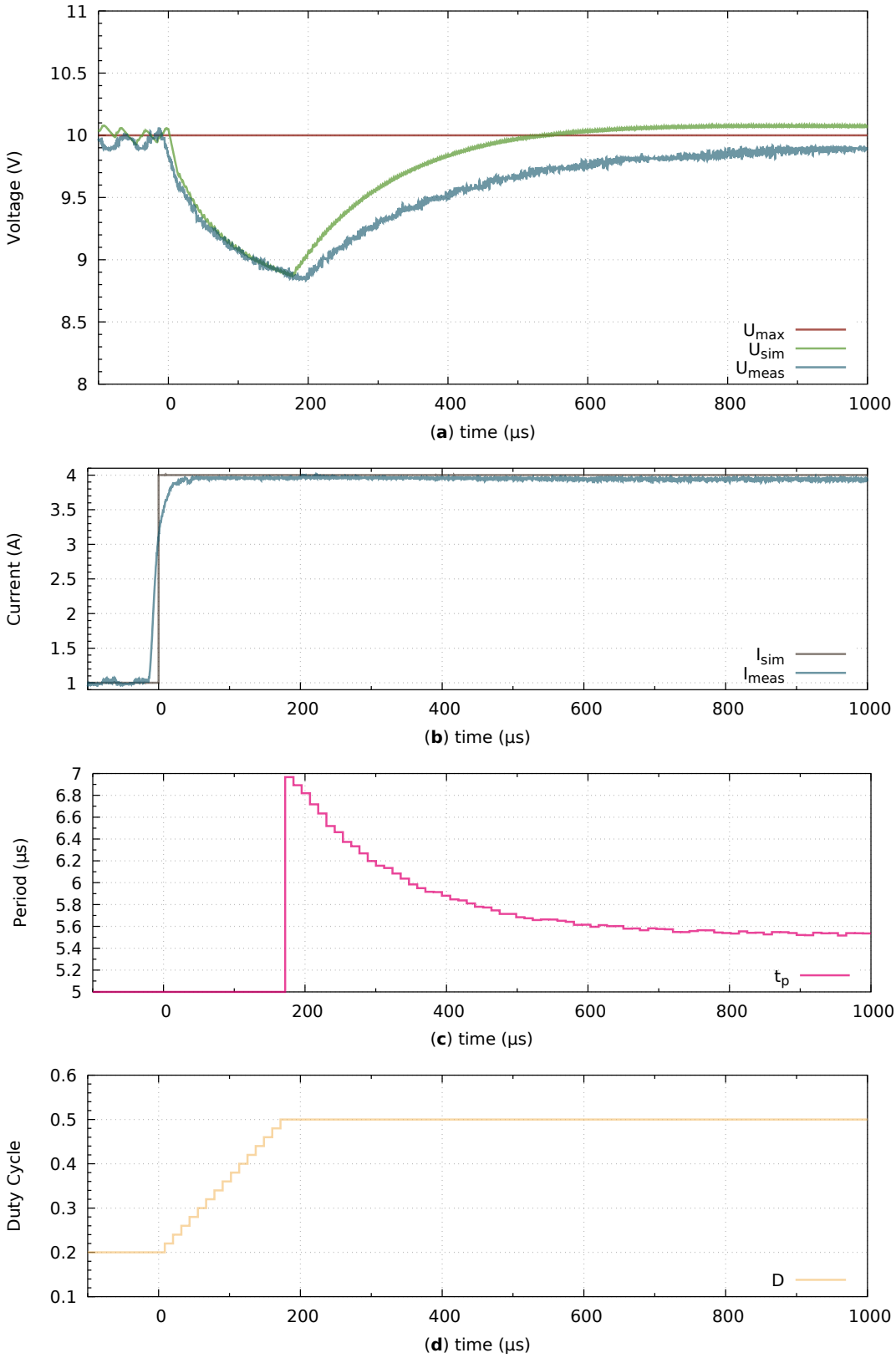


**Figure 10.** The load response of the power supply is measured: The external output current $I_{\text{out}}$ is increased from 1 A to 4 A (**b**) at $t = 0$. The output voltage is measured in (**a**), where an output voltage drop can be observed during duty cycle adjustment. The simulated output current is shown in (**b**), while the simulated switching period $t_p$ is shown in (**c**), and the simulated duty cycle $D$ is shown in (**d**).

### 5.5. CCCV Transition Step Response

In Figure 11, the constant current to constant voltage transition is measured. The effective output capacitance was determined to $C_{\text{out}} = 45\,\mu\text{F}$. The converter is first operated in constant current (CC) mode and then the transition to constant voltage (CV) is demonstrated. The CCCV control is implemented by choosing the minimal value of two parallel controllers, as it can be seen in Figure 3.

At $t < 0$, the converter operates in CC mode and the output current is limited to 2 A. The load $R_{\text{load}} = 10\,\Omega$ results in an output voltage of $U_{\text{out}} = 20\,\text{V}$. The voltage limit is set to $U_{\text{max}} = 24\,\text{V}$. After $t = 0$, the current limit $I_{\text{max}}$ is increased from 2 A to 3 A. The output voltage rises from 20 V within 400 µs to the output voltage limit of $U_{\text{max}} = 24\,\text{V}$. No output voltage overshoot can be observed. A consensus between simulation and measurement is shown.

### 5.6. Loop Gain Analysis

The loop gain analysis is conducted in simulation at an output voltage of 24 V and an amplitude of 0.1 V in CV mode. In Figure 12 a bandwidth of 1 kHz can be seen in the low acoustic noise design using a gain of 1/9. In a loop gain optimized design, using a factor of 1/4, a bandwidth of 3 kHz can be observed. The acoustic noise of loop gain optimized design can be seen as jitter in the magnitude.

Conventional LLC converters have a typical bandwidth of 2 kHz [7, p. 14]. Thus, the presented control has a similar bandwidth compared to a typical LLC converter.

The converters open loop gain in Figure 12 has a typical integrator characteristic and suggests the well tempered operation of the converter.

## 6. Conclusions

The paper demonstrates fast and accurate control of a series LC converter in constant current, constant voltage mode and reliable transitions between those operational modes. The target output current and voltage is reached in less than 400 µs during the step response test with 5% margin for large signals. In contrast to typical soft-switching power supplies, for example LLCs a large input and output voltage range can be achieved. Our prototype demonstrated an output voltage range from 0 V to 30 V. The previously proven high input voltage ripple rejection of the transfer function allows to replace electrolytic capacitors with film capacitors, significantly increasing the converters service life [1].

The CCCV characteristic allows the use of the converter for demanding applications, i.e. laboratory power supplies or lithium battery chargers. The CCCV control is made possible by a two stage design: The master controller sets the SLC current and the open-loop slave controller controls switching period, duty cycle and pulse skipping. The converter is stable over the whole operation range, from no load to heavy load conditions.

## 7. Patents

The modulation schemata by equation (1) is covered by a pending patent. The application number is not yet published.

**Author Contributions:** conceptualization, M. Heidinger; methodology, M. Heidinger; simulation, M. Heidinger; validation, Q. Xia; formal analysis, W. Heering; investigation, Q. Xia, M. Heidinger; writing—original draft preparation, M. Heidinger; writing—review and editing, C. Simon, F. Denk, S. Eizaguirre, W. Heering; visualization, Heidinger; supervision, R. Kling; project administration, R. Kling;

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## Abbreviations

The following abbreviations are used in this manuscript:

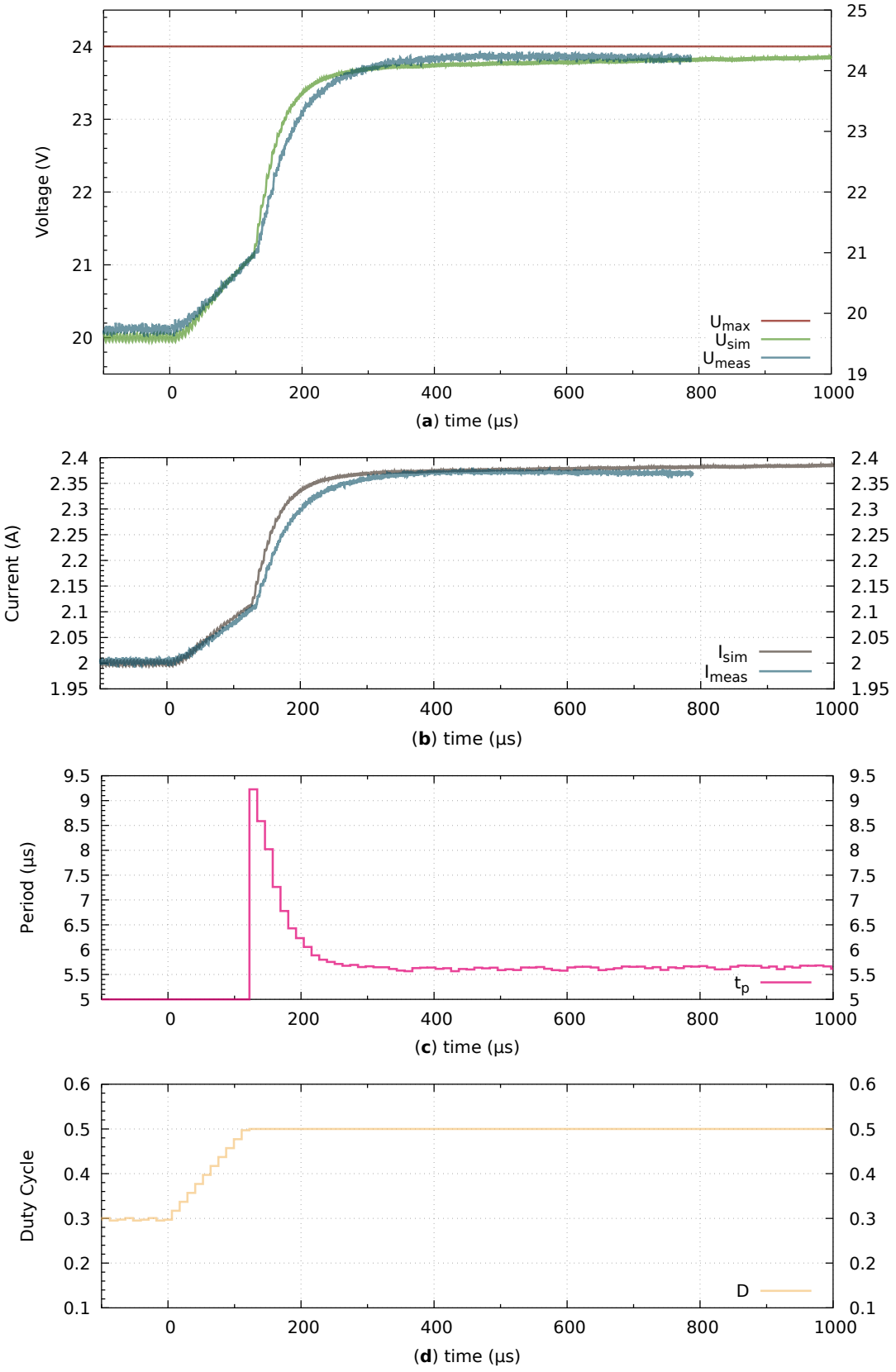


**Figure 11.** The constant current constant voltage operation of the control is verified: The maximal output current $I_{max}$ is increased in at $t = 0$ in a step response from 2 A to 3 A in (**b**) to demonstrate the CCCV behavior. The output voltage (**a**) limit is help constant at 24 V. Further, the measured and simulated output voltage are shown. The simulated switching frequency $t_p$ is shown in (**c**), while the simulated duty cycle is shown in (**d**).

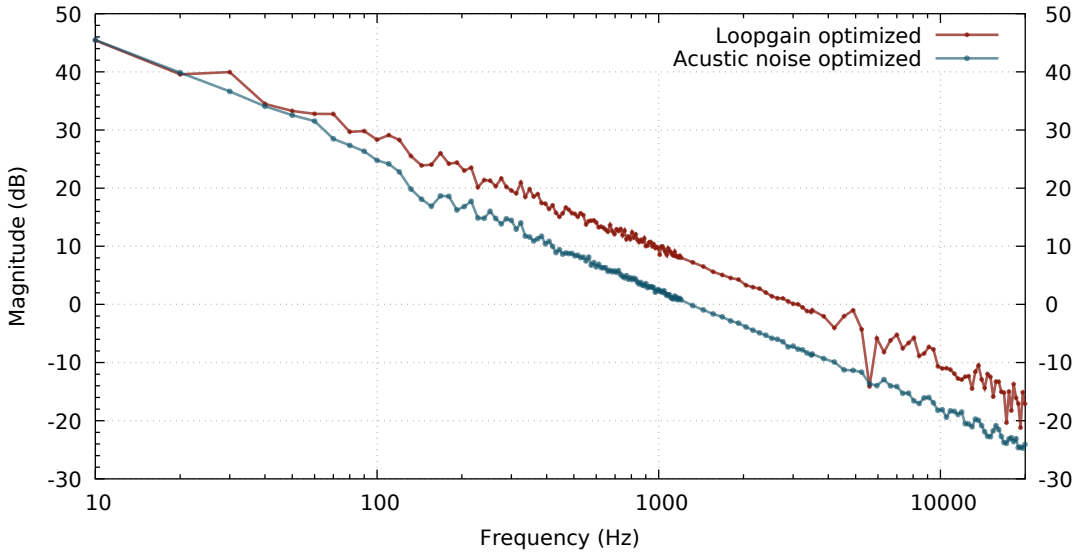


**Figure 12.** The simulated open loop gain magnitude over frequency is shown for two design choices. The worst case bandwidth frequency is larger than 1 kHz.

| | |
|---|---|
| CC | Constant Current |
| CCCV | Constant Current Constant Voltage |
| CV | Constant Voltage |
| DSP | Digital Signal Processor |
| MLCC | Multi Layer Ceramic Capacitor |
| PWM | Pulse Width Modulation |
| SMPS | Switch mode Power Supply |
| SL | Series LC (Inductor Capacitor) |
| SLCC | Series LC (Inductor Capacitor) converter |

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