The design of tunable photonic crystal biosensor with the integration of and PN phase shifter using PIC design approach

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Abstract—**Silicon based photonic integrated circuit (PIC) is a research focus in producing high density photonics. One of the potential applications of silicon PIC is the sensing and measurement system. In this work, we use the one-dimensional photonic crystal (1D-PhC) cavity design which and utilize it at the PIC level design. The 1D PhC design used as the compact model has the same characteristics as experimentally demonstrated in previous works. The compact model is made from the S-parameter extraction of the 1D-PhC device which is done by using Lumerical FDTD software. The PIC design integrates the 1D-PhC device as a sensing component with a PN-phase shifter (PN-PS) to function as a refractive index (RI) sensor calibration or tuning circuit. A custom design of PN-PS device is used by simulating and extracting the bias voltage-effective index (bias-Neff) data by using Lumerical DEVICE and MODE into the circuit simulator. The circuit level simulation is done by using Lumerical Interconnect software. Finally, we show the GDSII layout design of the 1D-PhC based photonic sensor calibration circuit with an analysis of generic silicon PIC design rules. The designed PIC is applicable for the bio-sensing applications and photonic SOC component. This work also shows the promise of PIC design approach for further PIC development.**

Keywords— Photonic compact model, silicon photonic integrated circuit (PIC), photonic crystal cavity refractive index sensor , tunable sensing circuit, photonic layout rules.

I. INTRODUCTION

Advanced biomedical trend such as personalized diagnosis requires the miniaturization of biomedical instruments. One of technology to realize this is the integrated design such as CMOS dan BiCMOS. However, for photonics-based design, traditional discreet photonics results in bulky and bigger instruments. The solution of this is the creation of photonic integrated circuit (PIC) design approach. The idea of PIC is driven by the already successful development of high-density electronics, particularly CMOS VLSI and the need for high-speed optical communication system and components [1], [2]. What makes this technology attractive is also because of the reusability of the CMOS fabrication infrastructure for the on-rising silicon photonic platform [2][3]. Thus, silicon photonics

has the potential for high density PIC and the development of photonic system-on-chip (P-SOC) [4].

To realize this complex system requires a proper set of design tools and design methodology. There has been an effort to develop the Silicon PIC design flows and tools [5], [6]. The developed Silicon PIC design flow utilizes a design flow similar with ASIC design flows particularly analog ASIC, which utilize the electronic design automation (EDA) tools consisting of three main levels: schematic design, layout design and design verification before it goes to tape-out. The complete silicon photonic design flow is shown in figure 1, which has been described in [5], [7]. In silicon photonics, a GDSII file format layout is usually made which is required for electron beam lithography (EBL) patterning process [8] during the fabrication phase.
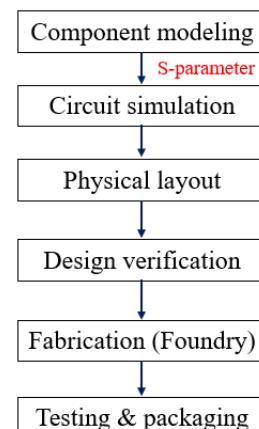
Fig. 1. Silicon photonic system design flow [5].

In usual electronics and photonics design flow, there is a part of creating a custom compact model of a designed device for circuit level simulation. The compact model can be made from the scattering parameter (S-parameter) extraction of the simulated device. In electronics, the S-parameter describes the response of an electrical or photonic device as a function of frequency. Experimentally, the S-parameter can be

characterized by using an electrical network analyzer (ENA) for an electrical device and optical network analyzer (ONA) for a photonic device [9].

The S-parameter data is an array of matrices containing the scattering data at its ports. It can represent how a device behave from a black-box point of view. A two ports device would have a 2 x 2 matrix for its S-parameter as illustrated in figure 2.

$$A_1 \longrightarrow \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \longleftarrow A_2$$
$$B_1 \longleftarrow \qquad\qquad \longrightarrow B_2$$
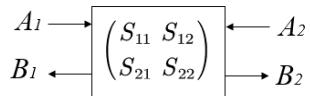
Fig. 2. An illustration of matrix for two-ports network

The full equation of the transfer matrix is given as follows,

$$\begin{pmatrix} B_1 \\ B_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} A_1 \\ A_2 \end{pmatrix} = S \begin{pmatrix} A_1 \\ A_2 \end{pmatrix} \qquad (1)$$

Where A_1 is the input light into the device through port 1, B_1 is the reflected light, and B_2 is the transmitted light. A circuit simulator usually simply solves this kind of matrix equations from component to component to get results.

In silicon photonics research, there has been a lot of research done on the device level photonics. Two main classifications of photonic devices are passive and active devices. The usual passive devices used in PIC design are photonic waveguide (photonic wire) [10], 90º bent waveguide [11], directional coupler [12], Y-branch [13], Mach-Zehnder interferometer (MZI) [14], [15], ring resonator [16] and Bragg grating [17], [18]. Ring resonator and Bragg grating are conventionally used for filtering and peak generation. The usual active photonic devices are first the modulator or tuner are usually PN-phase shifter [19], [20], micro-ring modulator [21] and thermo-optic phase shifter [22], and other important active devices are photodetector and laser. The main material for silicon photonic is silicon-on-insulator (SOI).

Because there have been a lot of researches at the photonic device level [23], the photonic devices research can be considered as matured at this time, although more new devices can be created as needed. The next step from the device level development is to go into the development of integrated-circuit level photonics that utilizes those developed photonic devices. This can be done by creating the compact model from any of previously developed devices.

Although previous PIC works are mostly for the optical communication system, there is also another need for developing PIC blocks for optical measurement system or SOC such as for bio-sensing system [24]. This is because photonic sensors are very sensitive which make it suitable for biosensor and micron scale detection. This paper focus on this application.

In our previous works, we have shown that the 1D-PhC sensor's output peak will shift on its wavelength when there is a change of its surrounding refractive index (RI) [25], [26]. 1D-PhC device has the advantage of having a sharp single peak characteristic as compared to the conventional Mach-Zehder

interferometer (MZI) device which can be designed at c-band wavelength and also accurately at 1550 nm [27], [28]. The sharp peak characteristic can be used as the sensing signal. It is also possible to use 1D PhC as one-port device, which utilizes the same path as the input and output [29].

However, biosensing measurement depends on a strict standard, so there is a need to calibrate the system for accurate measurement. The other factor that can disturb the accuracy of the measurement is the temperature influence. So, a tuner is one of the solutions that can be used for this issue.

In this work, we integrate the 1D-PhC biosensor with the PN phase shifter to make a tunable bio-sensing PIC. The 1D-PhC biosensor component can sense the different concentration of an analyte by sensing the RI change around its surrounding. The transmitted light signal from the 1D-PhC goes through the PN-PS component before goes out to the output coupler. If the RI inside the PN-PS is changed, the phase of the light signal which goes through it will be changed. This effect can be used to tune the resonance wavelength. The effect of RI change in crystalline silicon due to biasing voltage and charge carriers was first predicted by Soref and Bennett in 1987 [30]. Previous researches have shown the tunability of the resonance wavelength either by thermo-optic or plasma dispersion effect. In this work, the plasma dispersion effect is used to control the RI inside he PN-PS by controlling the applied bias voltage of the PN-PS.

The PIC design flow is followed to build a functional PIC schematic and final GDSII layout. The result from the 1D-PhC design shows that the resonance peak's wavelength will change when there is a change in the surrounding RI of the 1D-PhC. The result from the integrated 1D-PhC with PN-PS shows the shift of resonance peak when the PN-PS reverse bias voltage is increased. The results show the success of this work to design a tunable biosensing PIC which gives a miniature solution to tune or calibrate the biosensor for measurement accuracy.

II.   METHODOLOGY

Referring to the general silicon photonic design flow shown in figure 1, only the component modeling until physical layout design will be shown in this work. The design verification is done by comparing to specific design rules. Here. an analysis of the layout design with generic silicon photonic design rules will be discussed.

Before the design is started, the overall cross section of the designed chip will be identified in order to understand the circuit and the implementation of the physical layout design. The main material of the wafer used in this design is silicon-on-insulator (SOI), which is the standard material for silicon photonic. The cross-section of the most complex component used in this design, which is the PN-PS will be identified first because it contains almost all physical layers used in the design. The cross section of the PN-PS together with its interconnect components is shown in figure 3. Only PN-PS uses rib

waveguide in the circuit. The other photonic components in the designed circuit use strip waveguide.

All waveguides material is silicon. All waveguide's width is 500 nm. In the PN-PS design, the metal 2 (M2) connects the device from outside, which is from the electrical pad. M2 is connected to metal 1 (M1) through via 1 (V1). M1 is used for inside interconnect of the PN-PS and is connected to the Si rib waveguide through contact (CB). This cross section is identical as in the common CMOS IC design.

By seeing this most complex device's cross-section, we have seen most physical layers used in the layout design except the electfrical pad layer. Other additional layers in the layout design includes the doping regions of the PN-PS. The doping regions of the PN-PS will be shown later.
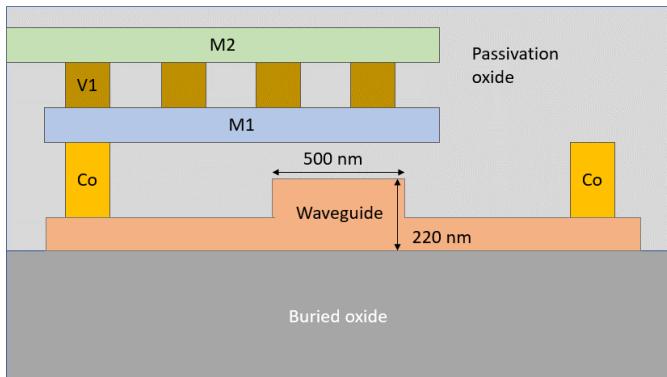
Fig. 3. The cross-section's view at PN-phase shifter as the most complex layers region in the PIC chip.

The objective of the design is to utilize the 1D-PhC device as the resonator and sensing element, then make the resonance wavelength tunable for calibration purpose. This can be done by integrating the 1D-PhC with the PN-PS device. The schematic design of the PIC is shown in figure 4.

The circuit uses ONA as both the light source and signal analyzer. The grating couplers designated as GC1, GC2 and GC3 are used as the coupling components to couple light into and out of the chip. Other than grating coupler, edge coupler can also be used. Utilizing the flexibility of PIC design, a reference output can be added to the circuit by splitting the input light by using a directional coupler (DC1). The reference output goes out through GC2. It can be also used as signal checker. Other than the directional coupler, a Y-splitter can also be used to split the light. However, a common Y-splitter will split the light equally into two direction, resulting in an unnecessary transmission loss for the main purpose. That is why a directional coupler is used here, which is only about 15% of light would be coupled across the directional coupler and goes to the reference output.

The data of the extracted S-parameter of the 1D-PhC device will be uploaded to the S-PAR component to make the 1D-PhC compact model. The waveguides length between the 1D-PhC

component is taken with the consideration of the final GDSII layout which will be shown later. Other than 1D-PhC S-parameter data, a specific data for the PN-PS component (PS1) must also be uploaded, which is the voltage bias-RI response data, rather than using the generic data in the circuit simulator. This is because we are not using a pre-designed model of the PN-PS for the final GDSII layout, so a custom design needs a thorough simulation to make sure the accuracy of the results, and the objective to design a tunable sensing PIC with manufacturing ready layout is achieved. Because the PN-PS is the most complex component and act as the controlling element in the circuit, it must be thoroughly designed and simulated. The PN-PS length is set to 1 mm, which is very long compared to the 1D-PhC device which is about 25μm long. The PN-PS will be connected to the electrical pads for biasing.
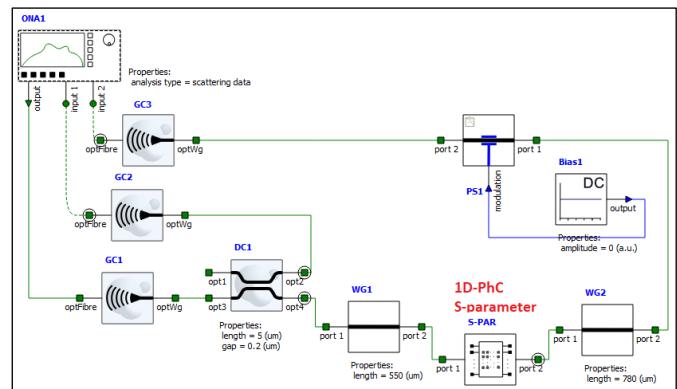
Fig. 4. The full PIC schematic for the tunable sensing circuit.

The design of the 1D-PhC which will be converted into the compact model is shown in figure 5. The 1D-PhC uses uniform holes of 50 nm radius (r), with the periodicity (a) of 400 nm, a cavity (c) of the length of 490 nm and number of holes of 50. The design parameters are chosen by understanding how the parameters change will affect the 1D PhC output and has been shown in the previous work [31]. The 1D-PhC structure will be simulated by using Lumerical FDTD software and the S-parameter will be extracted and transferred to Lumerical Interconnect for circuit level simulation.

Cavity

Fig. 5. The design of 1D-PhC used to make the compact model.

Next, the PN-PS device will be designed and simulated. A specific PN-PS structure will exhibit a different characteristic in term of the effective index response to the voltage bias (bias-Neff).

The width of the depletion region (W_d) of a PN-PS is given by [7],

$$W_d = \sqrt{\frac{2\epsilon_0\epsilon_S\left(V_{bi} - V\right)\left(N_A + N_D\right)}{qN_A N_D}} \qquad (2)$$

Where ϵ_S is the relative permittivity, V_{bi} is the built-in potential at the junction, V is the voltage bias, N_A and N_D are the doping

concentration of holes and electrons. Based on equation 2, two ways are known to increase the depletion width of a PN-PS can be which is by increasing the carriers' concentration by doping or increasing the bias voltage. In this PN-PS design, the doping concentration will be fix and the bias voltage will be varied to vary the depletion width. However, it should be noted that the change in voltage bias should change the carrier concentration at the pn-junction.

The change in RI at 1550 nm is described by the following equation [32],

$$\Delta RI = -5.4 \times 10^{-22} (\Delta N_D)^{1.011} - 1.53 \times 10^{-18} (\Delta N_A)^{0.838}$$

$$(3)$$

The doping region of the PN-PS rib waveguide is shown in figure 5. The doping concentration is 1×10^{18} cm^{-3} for n and p region, 1×10^{19} cm^{-3} for n+ and P+ region and 1×10^{20} cm^{-3} for n++ and p++ region. The PN-PS structure will be simulated using Lumerical DEVICE's Charge solver. The voltage bias of the PN-PS device is set from 0 to -20V. 20V is considered a high voltage for a chip application, but to realize the tunable sensing circuit, it is a reasonable value to be used. Lumerical DEVICE simulates the charge profile of the device, to get the effective index response, Lumerical MODE will be used by uploading the charge simulation data from Lumerical DEVICE. This bias-Neff result is an important information to show that the tunable circuit sensing will work as we want it to be. The specific bias-Neff response data will be transferred to Lumerical Interconnect.
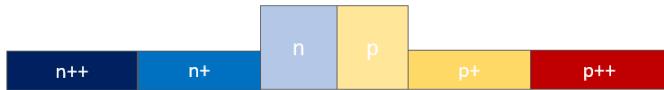
Fig. 5. PN-PS structure and the doping regions used in the simulation.

Finishing the device level design and simulations, all data which are the 1D-PhC S-parameter and bias-Neff data will be uploaded to the circuit schematic shown in figure 3, then the circuit will be simulated. The circuit simulation results should show that the tunable sensing PIC design objective is achieved, which output peak will shift when the bias voltage value is varied. Some of the components' value of the PIC schematic will be updated after the GDSII layout design is finished to make sure the accuracy of the results needed.

Finally, a GDSII format physical layout will be designed by using KLayout software. The designed GDSII layout will made for fabrication ready design. The designed GDSII layout in this work will be manually analyzed in according to generic silicon photonic design rules as stated in [7] and some rules are based on devices design. The waveguide routing will be done by using the open source SiEPIC toolkit. The components or cells which will be used in the GDSII layout are the combination of pre-designed library from SiEPIC process design kits (PDKs) and custom designed cells. The custom designed cells here are the 1D-PhC and the PN-PS devices.

III.   RESULTS AND DISCUSSION

The 1D-PhC device shown in figure 4 is simulated in Lumerical FDTD by using 2D FDTD solver with effective index value and S-parameter extraction setup. The transmission result of the 1D-PhC device is shown in figure 6, which shows a single peak output in the middle of a bandgap. The peak is at 1561.8 nm wavelength which is around the center of the targeted C-band wavelength. The normalized transmission value of the peak is 0.879, which means 12.1% of light loss at the peak and across the device. This amount of light loss should be considered for the final PIC design. The S-parameter data of the 1D-PhC is extracted and will be uploaded into Lumerical Interconnect for the PIC schematic simulation.
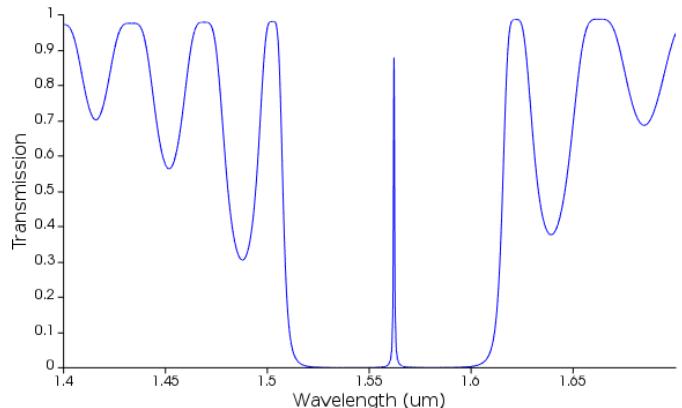
Fig. 6. The transmission of the 1D-PhC device simulated by using 2D FDTD solver with effective index method.

Next, the PN-PS is simulated in Lumerical DEVICE. The doping profile simulation is shown by figure 7. From the rib edge, the doping is gradually reduced from around 1×10^{20} cm^{-3}, to 1×10^{19} cm^{-3} and to 1×10^{18} cm^{-3}. Then, the simulation of the charge by varying the bias voltage and its effect to the depletion region is shown in figure 8. The result shows that as the bias voltage is increased in reversed from 0V to -20V, the depletion region width keeps increasing. This is the reason a higher reversed bias voltage which is until -20V is considered so that there are more changes to the guiding region of light mode which should change the effective index of the PN-PS waveguide.
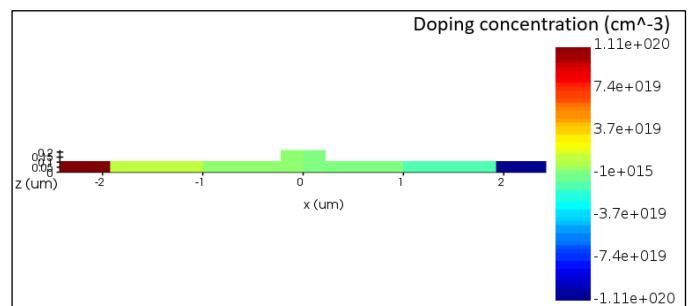
Fig. 7. The doping profile of the PN-PS.
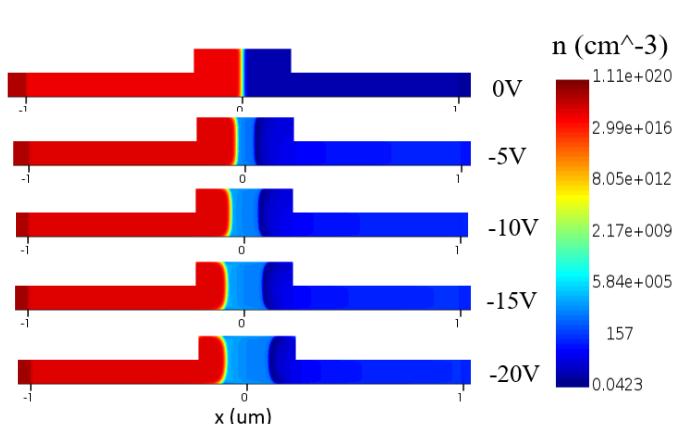
Fig. 8. Charge profile focusing at the center of the center of the PN-phase shifter. The depletion region at pn-junction increases as the bias voltage is increased.

To see the effective index change, the simulated charge profile data is uploaded to Lumerical MODE to simulate the rib waveguide with charge. Running the modal analysis, the result of refractive index profile can be seen. Figure 9 shows the comparison of imaginary RI profile of the uncharged waveguide for the PN-PS device (9a) and charged waveguide (9b). The imaginary RI in uncharged waveguide is zero while the imaginary RI in charged waveguide has a value. It shows the charged waveguide will exhibit some optical loss due to absorption [32]. Next, running the bias voltage sweep, the result of bias-Neff is shown in figure 10. It shows that the Neff increases in square root relation with the voltage. The change of Neff between undoped and charged PN-PS rib waveguide with bias voltage variation is shown in figure 11.
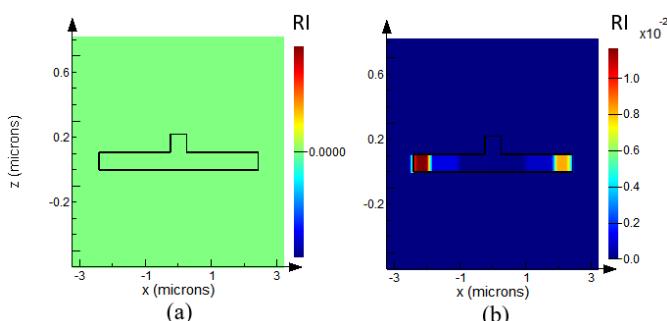
Fig. 9. Imaginary RI (loss) of (a) undoped waveguide and (b) doped waveguide
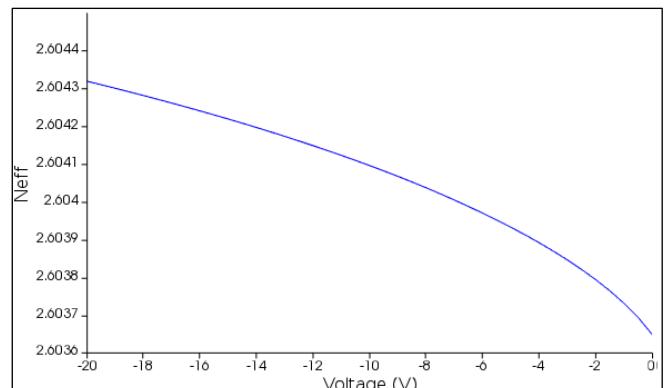
Fig. 10. Effect of bias voltage variation to the effective index of the rib waveguide for the PN-PS device.
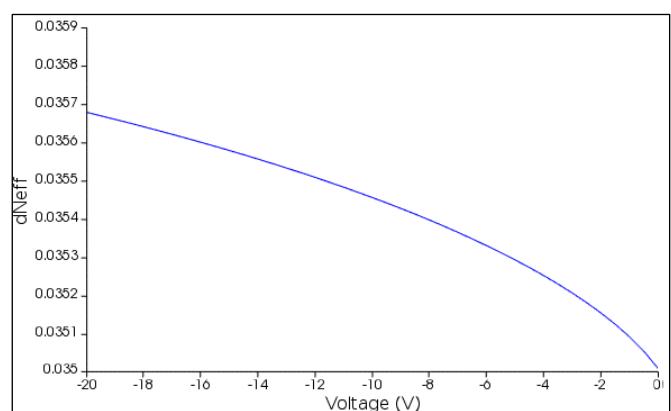
Fig. 11. The change of Neff between undoped and charged PN-PS rib waveguide with bias voltage variation.

With the finished simulation at the device level, the 1D-PhC's S-parameter and PN-PS bias-Neff data are now ready to be transferred to Lumerical Interconnect for circuit level simulation. The PIC schematic shown previously in figure 3 is now simulated. The simulation result of the designed tunable sensing PIC is shown in figure 12. The result shows the shift of the peak with by varying the bias voltage from 0 to -10 V as expected. Increasing the reverse bias voltage, the peak shows the redshift effect, which is going to the longer wavelength. However, as the reverse bias voltage increases, the peak's amplitude reduces.
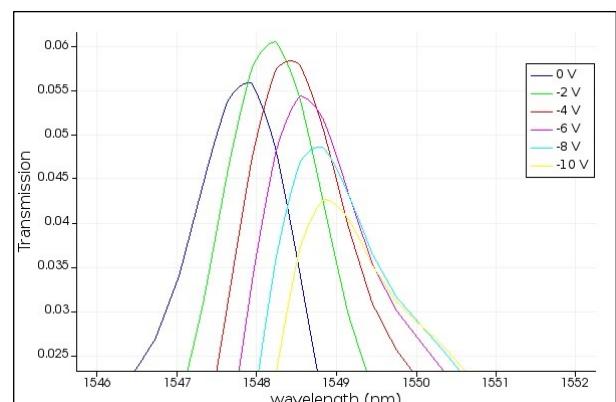
Fig. 12. The result of PIC schematic simulation shows that the wavelength of the peak signal can be tuned by varying the bias voltage of the PN-PS component.

The reducing amplitude of the peak is due to the absorption effect due to the changing concentration of charge carriers and has been described by the following equation. At 1550 nm, the change of the absorption (α) has been described by the following equation [7],

$$\Delta\alpha = 8.5 \times 10^{-18} \Delta N + 6 \times 10^{-18} \Delta P \qquad (4)$$

The absorption effect shows that the PN-PS can also be used for amplitude modulation application. However, since in this work only the wavelength tuning is needed, the reducing amplitude of the peak is considered a trade-off for the wavelength tuning.

Finally, the illustration of the fabrication ready GDSII layout is drawn as shown in figure 14. The layout follows a generic silicon PIC design rules. The main rule is about the spacing of the edge or grating coupler and the electrical pads which depends on the separation of the test probes. The grating couplers and the electrical pads in the layout are placed at different side because of the size of the test probes that would make it impossible to put both input and output components on the same side. The next rule is that the Si waveguide routings cannot be overlap because they are on the same layer. Then, the waveguide must be accurately aligned with the component's input or output. The waveguide bend will be of 5 μm radius as shown in figure 15 and as pre-set in routing setup. Finally, the metal wire routing requires that M2 layer to be used. M2 layer is needed for device interconnection because using M1 alone would be tedious for more complex PIC design.
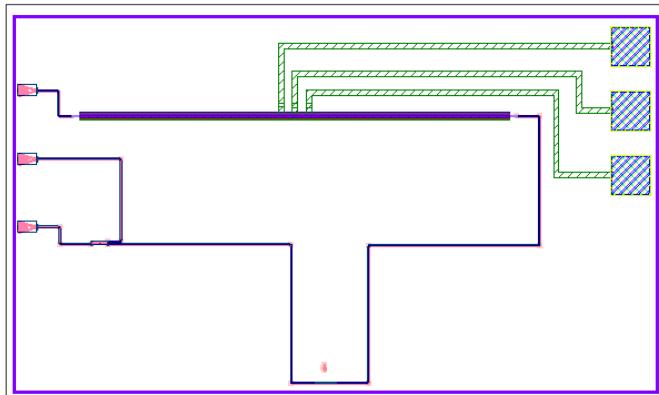
Fig. 14. The final GDS layout illustration of the designed PIC for prototyping, following the common silicon photonics technology design rules.
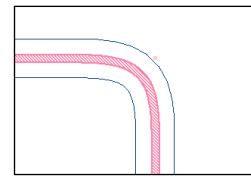
Fig. 15. The layout of waveguide bend with 5 um bend radius. The waveguide is surrounded by block fills.

The results of this research show the success of designing and simulating a tunable sensing circuit utilizing a 1D-PhC custom compact model integrated with a PN-PS device which is done by following silicon PIC design approach. The results also show the promise of PIC design approach to develop more circuits and blocks design to obtain a high-density PIC. Potential applications from PIC would be almost as same as electronics such as communications, sensing and measurement, computing, and others that are related. Right now, the combination of electronics and photonics chip to develop the SOCs is necessary. Using the same fabrication processes as CMOS, the co-design of CMOS-silicon PIC or the integration of it has huge potentials and more researches about this are needed.

IV.   CONCLUSIONS

We have designed and simulated a tunable sensing PIC by employing a 1D-PhC custom compact model which is not yet utilized at PIC level design. The design follows the silicon photonic integrated circuit design methodology. The 1D-PhC compact model is made from the S-parameter extraction of the device level simulation by using 2D FDTD solver with effective index value in Lumerical FDTD software. To realize the tunable sensing PIC, the PN-PS has been designed and simulated to extract the bias-Neff data by using the Lumerical DEVICE and MODE software and uploaded into the PN-PS compact model. The final PIC schematic with the uploaded data of 1D-PhC's S-parameter and PN-PS's bias-Neff has been simulated and the simulation result shows the shift of the peak signal as the bias voltage is varied. Finally, a GDSII layout has been designed analyzed by using generic silicon PIC design rules for fabrication purpose.

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