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Abstract: To build a stable power factor and high output accuracy, it should use balanced active and reactive power, also used ultrasonic PWM was used with the frequencies (20–500 kHz). I also used a three-phase dynamic load at the output system and was connected to the compound splicing (CS) system this is a novelty. An oscillator circuit with 4Ghz as a microcontroller is a novelty, and designing ADC is utilized to increase accuracy, as well as contribute to the reduction of loss brought on by the characteristics of voltage source inverters (VSI), such as dead time determined by the excess voltage or voltage drop in the inverter, circumstances abnormal to the load current, such as short circuit current in the production phase, and so forth. The innovation relates to the inverter's load sensing circuit, current smoothing during operation, reaction, spontaneous power factor enhancement of the inverter, and correction of reactive power of passive devices. This invention contributes to the advancement of D.C to A.C power converter by the achievement of extremely low losses, excellent precision, and lightweight construction. Additionally, the accuracy ranges from 99%, and the total harmonic distortion (THD) of the voltage and current is (0.1%-0.8%). We Power MOSFET are used, along with FPGA to improve control over the creation of ultrasonic PWM signals, the programmable peripheral interface (PPI) 8255A for regulatory work. The marks serve as proof of this.

Keywords: FPGA; PPI 8255A; oscillator circuit 4GHz; ultrasonic PWM; VSI.

1. Introduction

At this time, and we are in 2022, it has become obligatory to use provide high energy through the use of the switching frequency to reduce losses and increase accuracy, also through very fast switching frequency of turn-on and turn-off status. Therefore, the losses that occur in a MOSFET include studying the parasitic capacitance and the inductance. Consequently, must be taking into account the efficiency of the power electronic device, and the suggestions that show that most of the losses occur due to the plateau gate voltage and gate drive must be taken. From here, we start the process of changing and developing the work of an inverter. The MOSFETs have the characteristics of high accuracy and a few losses. Thereby, this is what distinguishes it from the other transistors, it features high gain current with high-frequency ability by switching process, It also has the advantages of linearity operation and more thermal stability through the switching of transitions, and is easily used on parallel because of the positive resistance factor [1–3]. Ultrasonic PWM makes to reduces the losses and increases accuracy in the inverter by syncretizing with increasing input voltage (Vin) and reducing the gate charge (QG) and thus reducing the gate resistance (RG). As well as, reducing parasitic capacitance (Cs), so that efficiency, accuracy, and low loss are achieved by other components such as using FPGA, PPI 8255A, and ADC, that will be used in this research.

1.1. Literature Review And Problem Statement

These papers (Bale et al; 2018) include improving the quality factor of the losses by distributing the energy inside a cavity it is used on the non-periodic matter with a frequency depth of 9.365GHz, as the obtained results were acceptable, noting that many researchers have researched similar to this work. The paper (Chen et al; 2019) proposal is to prevent the flux to the oscillator circuit by using an LC external circuit, that can be directly driven by a D.C transformer, the oscillating waves were not accurate because the ripple is not sufficient to prepare the oscillator circuit, in addition to the repetition process, there are successive distortions, and therefore we need continuity of work to obtain accuracy and few losses. The proposal is acceptable, but it needs minor changes to achieve work efficiency. In these papers (Gao, J., & Altintas, Y. 2019) it is proposed to use ultrasonic vibrations for cutting operations by controlling the resonance frequencies, that the cutting tests are not less than 30% efficient compared to drilling and milling operations. We believe that cutting operations need very high frequencies that exceed drilling operations and therefore need high voltages to create a condition of high-efficiency resonant synchronization. These papers (Gutierrez et al; 2018) it is proposed to study oscillators based on parity with a pulse generator where the proposal was to use an ADC and built on a VCO, it was proposed to improve the functioning o digital devices using a multi-stage modulator and built on a VCO-DAC, with an extended trance. The papers (Hertel, et al; 2016) The design for a 9-W class E resonant power converter in a 0.18-m CMOS technology is presented in this study. An extensive mathematical analysis of the self-oscillating gate drive that powers the converter is provided. To accomplish the proper phase shift necessary for zero voltage switching. The necessary spiral inductors were designed, and simulations at a switching frequency of 250 MHz show Q values as high as 14. A self-oscillating gate drive gives the converter an efficiency of 55%, according to simulations. The modeled inductor, however, presented problems when used with these.

2. Material and Method

One factor to improve output in this research is the use of ultrasonic PWM from $(20 - 500kHz)$ by using FPGA, which relied on the extent of voltage and the frequency from the sign utilized at the ultrasonic transducers, this is a novelty in this project, note that the FPGA is responsible for generating the signal with high accuracy. The choice of the frequency demand relies on the sort and the standard of required PWM [4]. Ultrasonic PWM is defined as the voice waves which set frequencies behind the domain of a person's hearing [5]. The chief standard in utilizing ultrasonic PWM is to ensure safe, to get high accuracy of the output power level, reduce the harmonic distortions (Low losses), and be more economical than the use of high frequency in an inverter, as well as used in the motor constant torque with speed variety by control of the amplitude of voltage and frequency to make to reduce torque pulsation in power switching.

The PWM effort can become rise till to undesired impact of the signals (harmonic distortion). The PWM efficiency and accuracy may be reductions occur if the used force is growing more than required without considering to components that may be used in the inverter. It can be concluded from the above paragraphs that controlling frequency, voltage, and power, as constant-time operation of the switching, have vital importance in designing ultrasonic PWM [6,7], with a high accuracy level on output and low losses through a design inverter. The proposal in this research is to use ultrasonic waves (UPWM) from (20 -500KHz) with the use of the positive phase sequence connected to compound splicing (CS) to improve the output with high accuracy and low losses, and control generation of UPWM by FPGA through field-oriented control (FOC).

Pulse is maximum generally used through actions about a pulse generator circuit to provide integrally the system of high accuracy ultrasonic PWM generators. As well as, an oscillator circuit used as a microcontroller with 4GHz is a novelty. in this study, an ultrasonic PWM generator system is designed by using an FPGA technology controller see Figure 1. The FPGA board is accountable for the reproduction of eight PWM digital signals into the lead for autonomous force operator collective programmable peripheral interface (PPI) type 8255A.

The hardware of this research includes digitally-controlled frequency and power units together by using an oscillator circuit proposed to control all the systems with the 4GHz.This proposed frequency has great benefits, including not to need use protection circuits from overcurrent and overvoltage that are excessive that cause surges that lead to damage to the device. As well as, reducing the size of the designed system.

The digital PWM signals obtained from FPGA implementation can securely and more reliably supply power to the MOSFETs in an inverter through the section for the ultrasonic PWM unit. The technical method used in an inverter changes the D.C. voltage to high-frequency waves through oscillator circuit control. Each three-phase transducer in the inverter has three ultrasonic transducers that have the same resonant frequency of nearly 100kHz. [8,9].

The remarkable thing is that every ultrasonic PWM can generate different frequencies, different powers, and at separate levels [10]. Therefore, when designing, we can use only one unit of FPGA, which is based on a field-oriented control (FOC). Transistors provide power conversion at ultrasonic frequencies greater than (20 kHz). If allowed develop DC/AC converters with higher accuracy or efficiency, higher power density, lower output voltage distortion, and lower spurious sign standards in the audio frequency group. The accuracy of the output voltage waveform would be better when the value of the frequency ratio is very large since the unwanted harmonics in the output waveform move to the higher frequency region. The ultrasonically-modulated inverters offer several technical and economic advantages compared with PWM inverters which are switched at frequencies of a few kHz, while the carrier frequencies of ultrasonic PWM are in the large of 20 kHz to 100 kHz. As well as, there are advantages to this high frequency which are: (1) Very low harmonic distortion in the PWM synthesized waveform, (2) minimal acoustic noise in an inverter resulting in quiet operation, and (3) A simplified modulator system can be used with the fixed carrier frequency. See Figures 1 and 2.
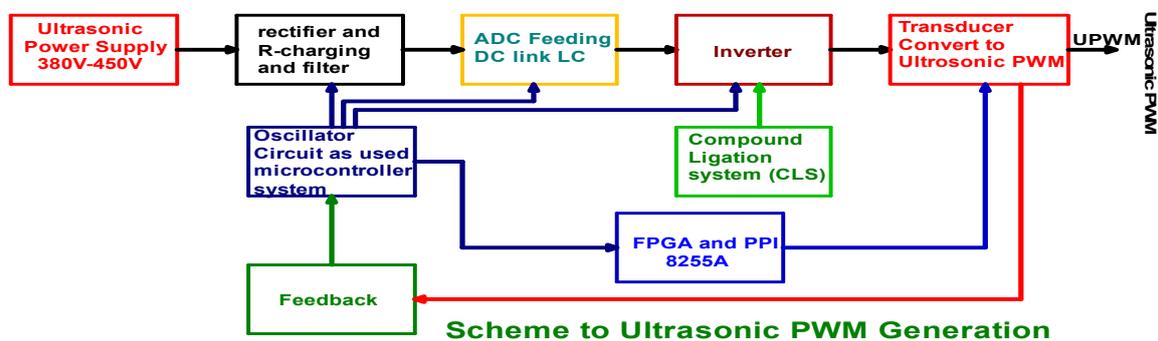

Figure 1. schematic diagram to illustrate the generation of an Ultrasonic PWM.

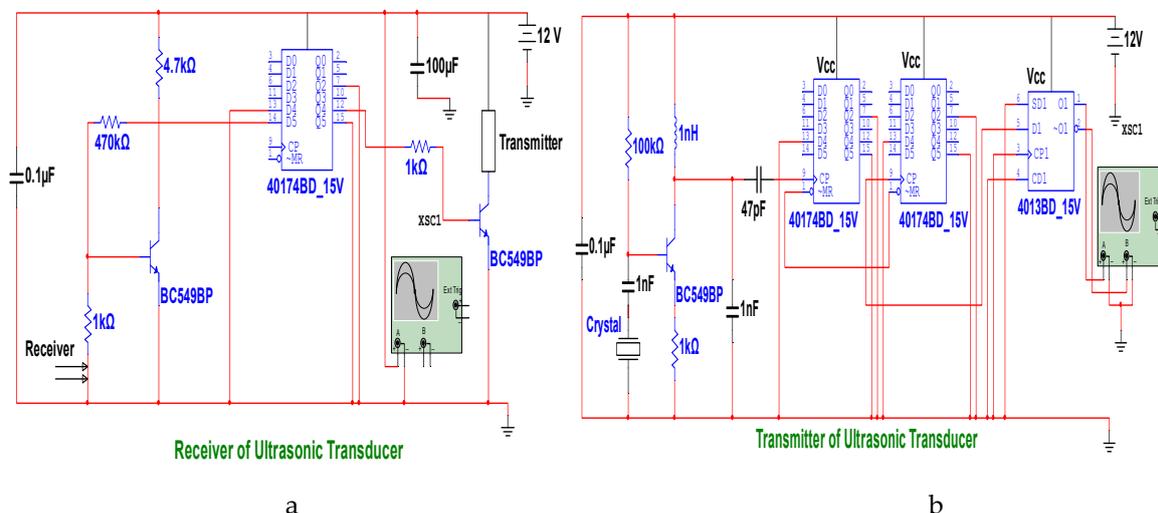a   b

Figure 2. shows the ultrasonic transducer; a-transmitter, b- receiver.

The second reason to improve production is to use compound splicing (CS) The foundation of the inverter's designed output filter is (LF, CF, and RL) [11], When designing, it is important to minimize total harmonic distortion (THD) and ripple voltage (RV) at linear and nonlinear rectifier (RC) loads. Given its importance, the design of the filter has a very important role in reducing losses and increasing output accuracy, and it is considered a new work in conjunction with a positive phase sequence. The total of the values of the reactive power (Q) that can be produced in the inductive and capacitive filter is indicated by (LF, and CF), which should have required egalitarianism of interacting power coefficients.

$$L_f = \sqrt{\frac{1}{M}\left(\frac{1}{f_s}\right)}\, R_L \ and \ C_f = \left(\frac{1}{f_s}\right)\left(\frac{1}{R_L}\right) \tag{1}$$

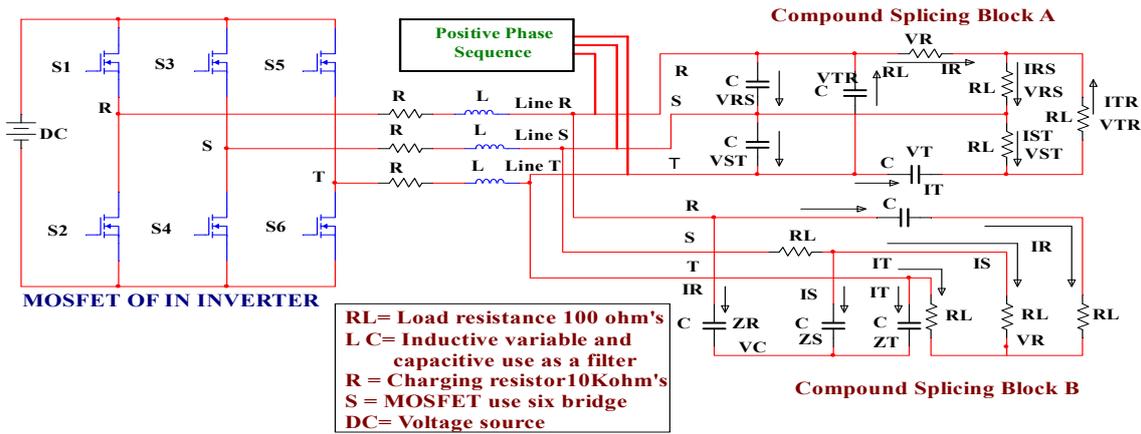Where, R_L: is the load resistance, f_s: is the switching frequency, M: is the modulation index.

Figure 3. Graphic outline of compound splicing attached with the inverter.

$$L_f = \left(\frac{1}{3}\right)\left(\frac{1}{f_s}\right) R_L \ and \ C_f = \left(\frac{1}{f_s}\right)\left(\frac{1}{R_L}\right) \tag{2}$$

The compound splicing (CS) of balance load which is displayed in Figure 3A,B) displays 4 lines egalitarian to PWM.

$$L_f = \left[\left[\sqrt{\frac{1}{M}\left(\frac{1}{f_s}\right)}\, R_L\right] // \, [\left(\frac{1}{3}\right)\left(\frac{1}{f_s}\right) R_L]\right] \ and \ [\ C_f > \left[\left(\frac{1}{f_s}\right)\left(\frac{1}{R_L}\right)\right]] // \, [\left(\frac{1}{f_s}\right)\left(\frac{1}{R_L}\right)] \tag{3}$$

Ultrasonic PWM is advantageous for reducing the ripple voltage's (RV) amplitude, depending on the passive components employed. Given that the inductance serves as the current source, an excess current will mostly flow through the capacitor's (CF) filter, raising the output voltage. Therefore, it would appear that cutting would take longer in an inverter than switching (ON-OFF), thus overtaking would be similar to the open circuit's work [12,13]. The output voltage controller's accuracy is at its highest for tiny modulation indices (M) due to the potential for a rise in the primary harmonics of an inverter output voltage that could result from (1-M) VDC. For lower productivity filter inductances, we should have a modest modulation index (M) so that the voltage controller in use is accurate enough. The voltage value above the filter inductor must be greatly raised when a nonlinear rectifier RC load starts to operate and pulse current starts to flow to the load capacitor. From equation (4), M appears at an extreme worth that is constrained [14].

Controlling the modulation index (M) is one method for boosting voltage gain (Hertel et al; 2018), however doing so alters the duty cycle, which impacts losses. in this state, we must manipulate the (1-M) base, which has the potential to result in current ripples at low frequencies, to generate PWM with a significant jump in duty cycle support.

$$M_{max} < \frac{\sqrt{3}}{2} / (\frac{W_m L_f}{R_S} + \frac{\sqrt{3}}{2}) \tag{4}$$

That the compound splicing (CS) in block A employs a portion of capacitors to define the redistribution of active power among the phases and compensate for most of the load's reactive power, also in part B the capacitors compensate for the active and reactive power on the other side, the crew load compensator can achieve the appropriate power factor and total stability. Contrary to the conventional compensation method, this is the new best technique. It will result in small size, reduced costs, elastic control, high accuracy (99%), and extremely low losses (0.11%). The correctness of the system is observed using the MATLAB, Simulink application. It has been found that the system's precision and low losses depend on passive components; this depends on UPWM, and the compounds of (LF, C F, and RL) change in value in response to ultrasonic PWM. Table 1., makes it evident that the values of the passive components (CL, LF, and RL) depend on the accuracy and losses of the ultrasonic PWM signal.

Table 1. Shows the rapport between low loss and ultrasonic PWM.

Ultrasonic PWM (kHz) (UPWM)	CF (Farad)	LF (Henry)	THD V&I %
20	2.0×10^{-6}	1.0×10^{-3}	0.1%
25	2.5×10^{-6}	1.0×10^{-3}	0.8%
27	2.6×10^{-6}	1.2×10^{-3}	0.2%
30	2.0×10^{-6}	2.8×10^{-3}	0.1%
36	2.7×10^{-6}	4.6×10^{-3}	0.3%
39	2.5×10^{-6}	2.6×10^{-3}	0.8%
40	2.2×10^{-6}	3.0×10^{-3}	0.9%
43	2.6×10^{-6}	3.2×10^{-3}	0.4%
50	2.4×10^{-6}	3.2×10^{-3}	0.6%
51	2.4×10^{-6}	3.2×10^{-3}	0.7%
60	2.5×10^{-6}	3.5×10^{-3}	0.6%
70	2.4×10^{-6}	3.8×10^{-3}	0.6%
80	2.2×10^{-6}	2.8×10^{-3}	0.4%
90	2.7×10^{-6}	2.9×10^{-3}	0.1%
100	2.7×10^{-6}	3.9×10^{-3}	0.3%
120	4.4×10^{-6}	5.0×10^{-3}	0.2%
135	4.6×10^{-6}	5.2×10^{-3}	0.1%
140	4.8×10^{-6}	5.4×10^{-3}	0.1%
450	5.0×10^{-6}	5.8×10^{-3}	0.1%
500	5.2×10^{-6}	6.2×10^{-3}	0.1%

Due to the triple harmonics that result from the neutral point's incidence, an inverter's PWM needs to be modified [15]. For voltage and current variables, A balanced load of matrices was shown in equation (5).

$$[X_1 \ X_2 \ X_3]^T = [X_{1k} \cos wt \ X_{2k} \cos(wt - 120^0) \ X_{3k} \cos(wt - 240^0)]^T \tag{5}$$

The constant and sync framing $\alpha\beta$ is offered by converting the matrix as follows:

$$[\alpha\beta - positive] = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix}^T = [\alpha\beta - negative]^{T-} \tag{6}$$

Where: ω is the grid frequency, $\alpha\beta$ is the evidence of the constant shape, and the positive and negative shapes (voltage and current) denote the series of synchronous shaps in the positive sequence voltage.

$$\begin{bmatrix} i_{RS} \\ i_{ST} \\ i_{TR} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} iR - iS \\ iS - iT \\ iT - iR \end{bmatrix} + \begin{bmatrix} i_r \\ i_r \\ i_r \end{bmatrix} \tag{7}$$

Where: The positive-phase sequence is signified in [$i_r = I_o \cos(\omega t + \gamma)$]. The relation between line-to-line voltage and a neutral point for the grid is specified via the following:

$$\begin{bmatrix} V_{RS} \\ V_{ST} \\ V_{TR} \end{bmatrix} = \begin{bmatrix} V_{RO} & - & V_{SO} \\ V_{SO} & - & V_{TO} \\ V_{TO} & - & V_{RO} \end{bmatrix} \tag{8}$$

The voltage control of the DC abilities depends on the equipped input design. The immediate and medium energy losses worth are calculated as follows.

Positive sequence voltages:

$$\begin{bmatrix} P_{RS} \\ P_{ST} \\ P_{TR} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \frac{1}{2}V_{\bar{q}} & +\frac{\sqrt{3}}{2}V_{\bar{d}} & \frac{\sqrt{3}}{2}V_{\bar{q}} - \frac{1}{2}V_{\bar{d}} \\ -V_{\bar{q}} & 0 & V_{\bar{d}}\,0 \\ \frac{1}{2}V_{\bar{q}} & -\frac{\sqrt{3}}{2}V_{\bar{d}} & -\frac{\sqrt{3}}{2}V_{\bar{q}} - \frac{1}{2}V_{\bar{d}} \end{bmatrix} \begin{bmatrix} i_q \\ i_d \end{bmatrix} \tag{9}$$

Negative phase sequence voltages:

$$\begin{bmatrix} P_{\overline{RS}} \\ P_{\overline{ST}} \\ P_{\overline{TR}} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \frac{1}{2}V_q + \frac{\sqrt{3}}{2}V_d & \frac{\sqrt{3}}{2}V_q - \frac{1}{2}V_d \\ -V_q\,0 & V_d\,0 \\ \frac{1}{2}V_q - \frac{\sqrt{3}}{2}V_d & -\frac{\sqrt{3}}{2}V_q - \frac{1}{2}V_d \end{bmatrix} \begin{bmatrix} i_{\bar{q}} \\ i_{\bar{d}} \end{bmatrix} \tag{10}$$

It might note from equation (8) that they are not stable, and based on this, the proposition utilized in the search is to locate the duration of the switching frequency by mutable the worths of the Lf, Cf. thus the duty cycle of ultrasonic PWM is controlled, and after that, these worths can fulfill demands for high accuracy and low losses.

$$\begin{bmatrix} P_{RS}^{LC} \\ P_{ST}^{LC} \\ P_{TR}^{LC} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \frac{3}{2}V_q + \frac{\sqrt{3}}{2}V_d + \frac{3}{2}V_{\bar{q}} + \frac{\sqrt{3}}{2}V_{\bar{d}} & \frac{\sqrt{3}}{2}V_q - \frac{3}{2}V_d - \frac{\sqrt{3}}{2}V_{\bar{q}} + \frac{\sqrt{3}}{2}V_{\bar{d}} \\ -\sqrt{3}V_q^+ - 3V_d^- & -\sqrt{3}V_q^+ + 3V_d^- \\ \frac{-3}{2}V_q + \frac{\sqrt{3}}{2}V_d - \frac{3}{2}V_{\bar{q}} + \frac{\sqrt{3}}{2}V_{\bar{d}} & \frac{\sqrt{3}}{2}V_q + \frac{3}{2}V_d - \frac{\sqrt{3}}{2}V_{\bar{q}} - \frac{\sqrt{3}}{2}V_{\bar{d}} \end{bmatrix} \begin{bmatrix} i_{LC}\cos\gamma \\ i_{LC}\cos y \end{bmatrix} \tag{11}$$

The power of every phase is 1 to 3 of the gross energy production. The Clark transformation is signified as follows.

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}, \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{12}$$

The merit of utilizing αβ and dq in the constant shape is to disconnect axes from a mutable, the control of the constant shape is carried out via the phase shift by (90⁰) of two sine waves, with the reference voltage, but be an obstacle when the reference voltage is unsteady with frequency. Park transformation at constant αβ and dq wording also uses ωk as the angular basic frequency of the output.

$$P^{-1} = P_{x\alpha\beta,dq}^{-1} = \begin{bmatrix} i_{Lf,\alpha,d} & i_{Lf,\beta,q} & V_{o,\alpha,d} & V_{o,\beta,q} \end{bmatrix}^T \tag{13}$$

Lastly, power equations signal that the balance of the product is caused via the balanced of LF, and CF, by the alterations that amount are restricted, thus, the synchronous UPWM with active of FPGA, filter design, and microcontroller by an oscillator circuit, gave positive results through high accuracy and low losses.

The third factor to improve output is the design of the ADC circuit was used to control the output by determining the value of the input voltage as well as to maintain the continuity of the voltage flow to the LC tanks in conjunction with the inverter work and thus it enhances the work of the MOSFET through the continuity of the voltage flow regularly, in addition to feeding the FPGA in digitally of bits sequentially [15]. Thus ADC transforms voltages through a few input bandwidths, and it rejects distortion in high frequencies, also its work is slow. It is characterized by its high accuracy through fastening of modulation frequency at 50Hz or 60Hz, a little current is used and it is desirable in different uses [16]. See Figure 4.
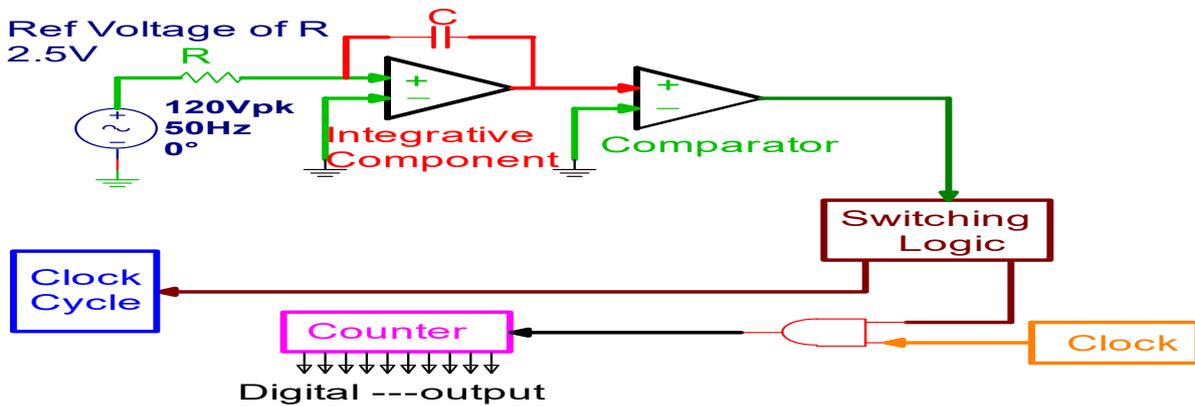
Figure 4. Block diagram of dual-slope ADC.

The dual-slope of the ADC circuit through Figure 4, is comprised of logic switching, an integrator circuit, comparator it works as a comparison between the input voltage and the reference voltage. The clock cycle, displays the time needed to measure the input voltage, the unknown voltage identified in the integration circuit and it represents the reference voltage. The switching works by the difference between the measured voltage and the reference voltage. The process is repeated by the integration circuit by unloading the capacitor charge bound in parallel with the integrator component. The conversion of the dual slope is in two stages, the first is run-up, which is called the (counting up) phase, and the second stage is run-down, which is called the phase (counting down). Through run-up, the provider of voltage to the integration component by the input voltage, in this case, the voltage supply of the integration component is chosen by the switch of action. Then, the integration components permit charging the capacitor for a specified period, for the run-down, the input voltage to the integration component is through reference voltage, i.e. the voltages are negative, and the reference voltages value is chosen by the integrator component based on to the switch devices. The integrator time of the output unit in this phase is zero. When the input voltage value is constant, the integrator component output appears in the following equation. [16,17].

$$V_0 = \frac{V_{in}}{RC}(T_{int} + V_{int}) \tag{14}$$

$$V_i = -V_{ref}\left(\frac{T_d}{T_{up}}\right) \tag{15}$$

Where: Vo is the output voltage, Vref is the reference voltage, Vi is the input voltage R and C, is the resistor and capacitor, V_{int}, initial supplied voltage, T_{int}, initial time.

The fourth factor in improving the output is the use of 4GHz frequency in the oscillator circuit to control the operation of the system without the need for external control components. This leads to a small size of the device, high accuracy, and low losses through the use of an external LC circuit, and RL slow charging circuit to increase the accuracy of the inverter work and increase the control. See Figure 5.
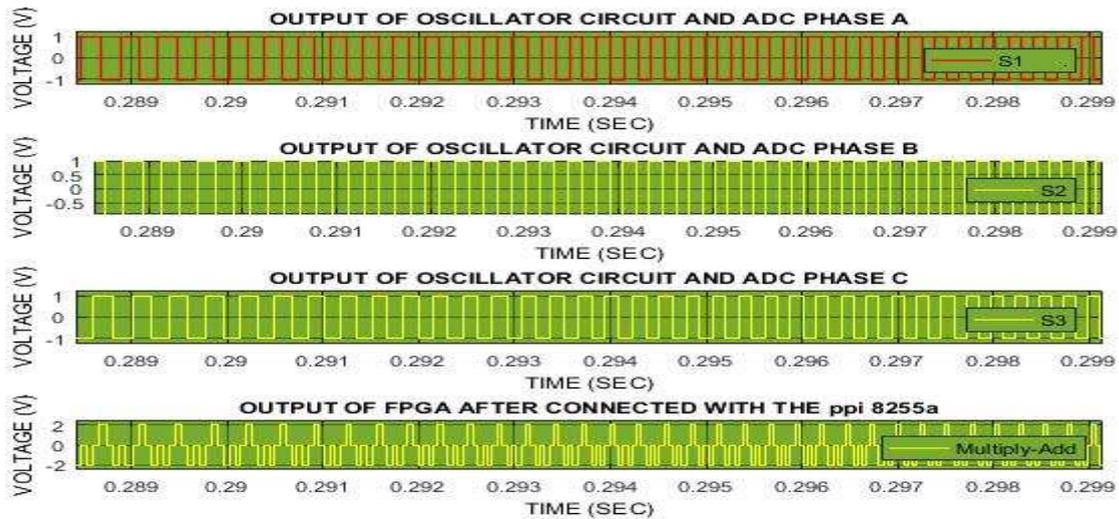
Figure 5. Output of the oscillator circuit and FPGA after connected with the PPI 8255A.

3. Results and Discussion

The oscillator circuit used a clock frequency of 4GHz, in this case, all the operations of an inverter are controlled in real-time, the design of the Ultrasonic PWM inverter system uses the frequency ratio changing technique to use minimize the unwanted harmonics. Through the results in Table 1., note the effectiveness of the passive components in generating ultrasonic PWM in the output system, note when 20kHz, 30kHz, and 90kHz been obtained a high accuracy is 99%, and few losses of THD is (0.1% → 0.8%), this is meaning that the medium energy of switching losses (EMS) is low, as the switching losses depend on the input voltage (Vi) and output of current (Io), as well as the switching frequency (fs) and time that determines the work of switching between turn-on (t2+t3) and turn-off (t5+t6). See equation (16), and see Figure 6.

$$E_{MS} = \frac{1}{2}(V_i I_o)(t_{on} + t_{off})(f_S) \tag{16}$$

Where: EMS is the medium energy of switching losses, fs is the switching frequency.
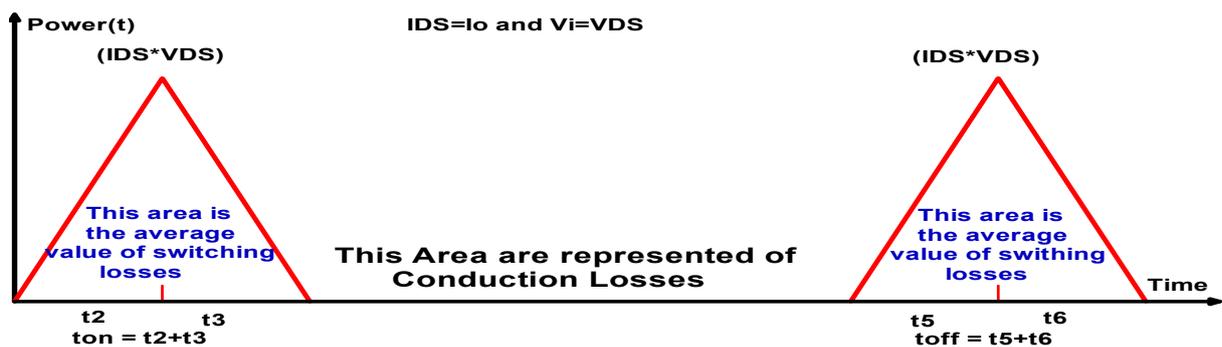
Figure 6. Diagram of power losses of the MOSFETs in an inverter (EMS and EMC).

medium energy of conduction losses (EMC) is tiny because it depends on the output current (Io), RDS is the resistance of drain-source of a MOSFET, and duty cycle. see equation (17)

$$EMC = I_o^2 * R_{DS} * D \tag{17}$$

$$E_{on} = ID_{on} * VDD * \left(\frac{tri + tfv}{2}\right) \tag{18}$$

Whereas $t_{on} = tr_i + tf_V$

Where: E_{on} energy in a turn-on, ID Drain current in a turn-on, VDD Drain voltage in a turn-on, tri rise time of current in a turn-on, and tfv fall time of voltage in a turn-on

$$P_{on} = E_{on} * f_s \tag{19}$$

If VGS is very small thus the energy off is:

$$E_{off} = ID_{on} * VDD * \left(t_{off}/2\right) \tag{20}$$

Whereas $t_{off} = tr_V + tf_i$

$$P_{off} = E_{off} * f_S \tag{21}$$

We conclude from equation (16). This raise in the switching frequency results in a rise in the medium energy switching losses. The medium switching energy loss is relying upon turn-on and turn-off periods, and the medium switching losses is too rely on the switching frequency, While, the conduction losses of equation (17) rely on the duty cycle (D).

The principle treatment that has been worked on in this research is to raise the ultrasonic PWM value from (20kHz-500kHz), to reduce losses and increase accuracy in conjunction with the compound splicing of output via the use of positive phase sequence to compensate for the losses that may occur from the generation of the magnetic field due to increasing the current in the inductance, and thus the generation of the parasitic capacitance, which leads to a occur a high degree of heat and increase the RDS(ON), and after that works to stop the inverter. Also, the design of the ADC gave an impetus to control the input voltage and compare it with the reference voltage, and thus the distortion was controlled to the very smallest possible value.

That utilizing the UPWM from (20—500khz) to acquire the necessary power and the voltage and current between phases, it has become an urgent necessity to improve the work of the inverter in this project thus positive voltage sequence, was employed at active power (P) of 6KW and reactive power (Q) of 3KVAR. Demonstrates that compound splicing using the three-phase dynamic load and synchronous with ultrasonic PWM and FPGA to produces high accuracy and low losses. Knowing that the three-phase dynamic load has been modified in the frequencies (120-500kHz) to an active power (P) of 8KW and a reactive power (Q) of 6KVAR at the frequencies of 120 kHz, 135 kHz, 140 kHz,450 kHz, and 500 kHz to acquire the necessary power, were to extend the period of switching frequency for to avoid interference between current and voltage, see Table 2.

Table 2. Shows the relationship between the ultrasonic PWM and generated voltage, current, positive sequence voltage, active power (P), and reactive power(Q), these results depend on the passive components (CF, LF, and RL).

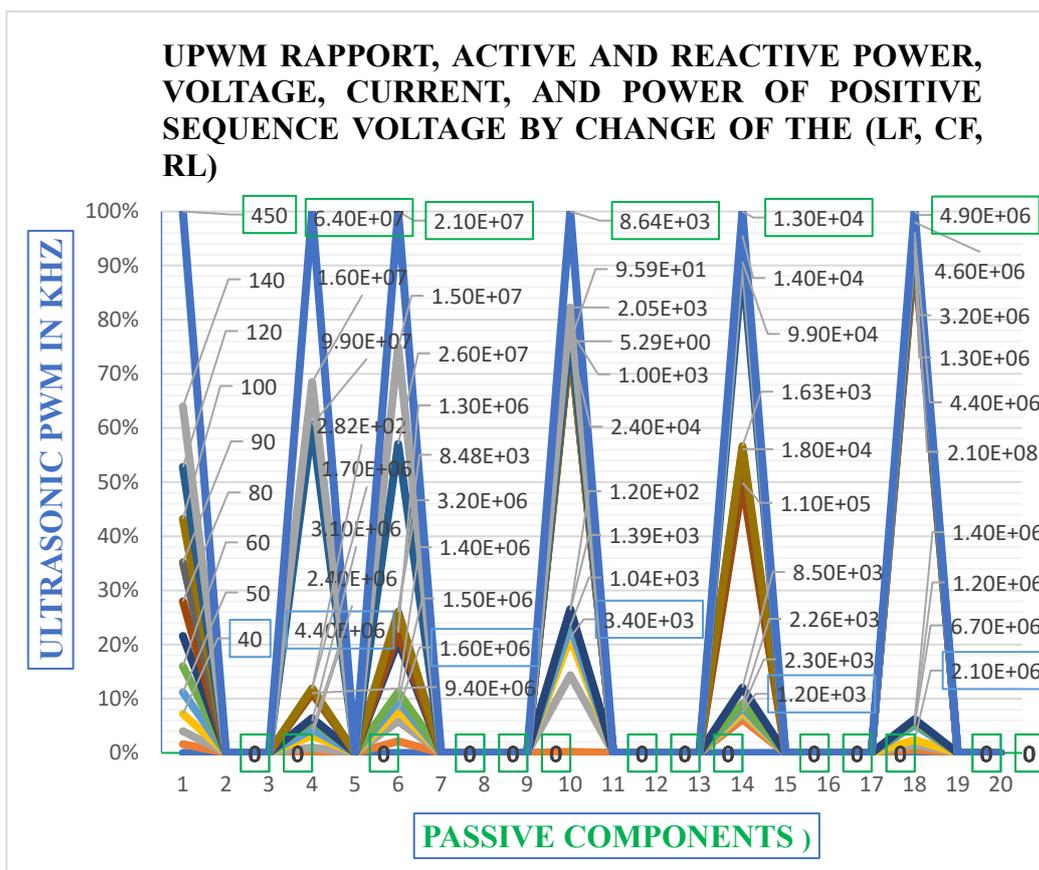| Ultrasonic PWM (kHz)	Active Power (W)	Reactive Power (VAR)	The voltage between phase to phase (V)	The current between phase to phase (A)	Positive sequence voltage in (W)
20	1.5×10^5	1.8×10^5	1.0×10^2	1.8×10^3	1.4×10^6
30	1.2×10^6	1.9×10^6	8.6×10^3	2.4×10^3	2.2×10^7
40	5.3×10^6	1.8×10^7	9.3×10^3	5.2×10^3	4.2×10^7
50	6.8×10^7	1.1×10^7	9.4×10^3	5.2×10^3	5.0×10^7
60	7.7×10^7	2.0×10^7	9.41×10^3	5.3×10^3	5.1×10^7
70	8.9×10^7	7.8×10^7	5.7×10^4	6.1×10^3	5.5×10^7
80	9.4×10^7	1.3×10^8	6.4×10^4	6.3×10^3	1.1×10^8
90	1.7×10^8	3.2×10^8	9.1×10^4	1.8×10^4	1.3×10^8
100	2.7×10^8	4.0×10^8	9.2×10^3	2.4×10^4	3.2×10^8
120	3.3×10^8	4.5×10^8	9.7×10^3	5.7×10^4	3.4×10^8
135	8.5×10^8	4.9×10^9	4.94×10^4	5.8×10^4	3.6×10^8
140	9.7×10^8	5.3×10^9	5.6×10^5	6.1×10^4	4.6×10^8
450	9.92×10^8	6.1×10^9	2.8×10^5	7.4×10^4	6.5×10^8
500	9.2×10^8	2.6×10^9	3.0×10^4	2.8×10^4	6.8×10^8

Figure 7. Shows the values of UPWM, active power, reactive power, voltage, current, and the power of positive sequence voltage by the change of the passive components.
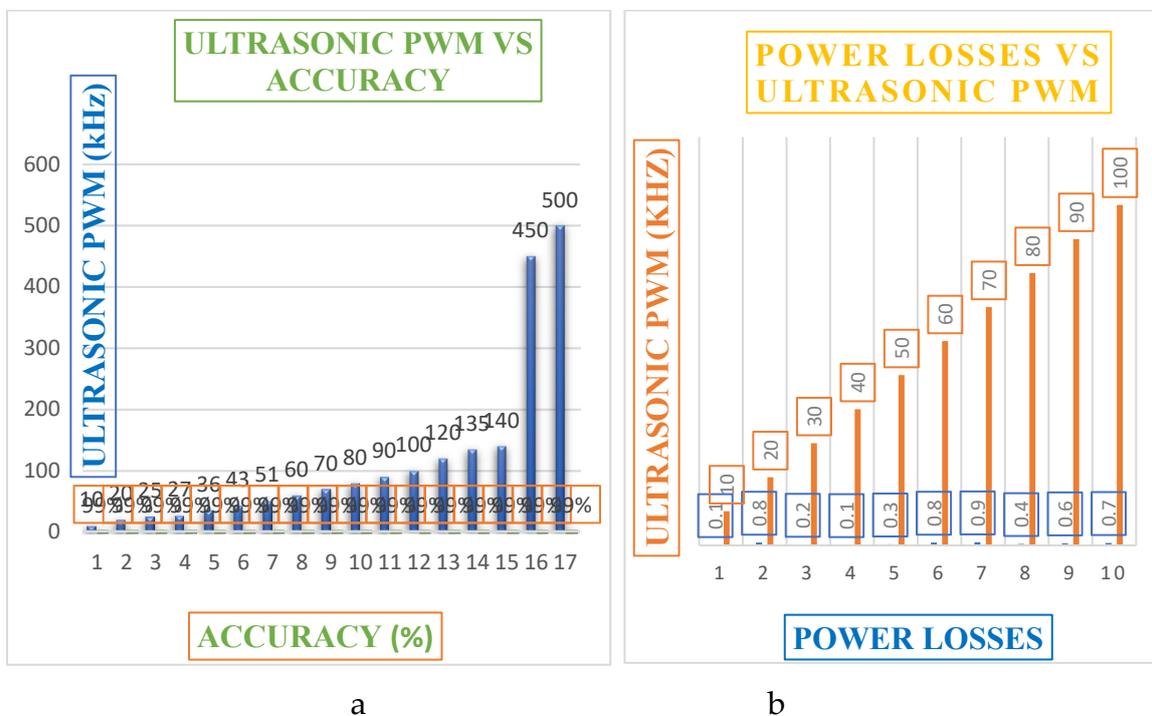

a   b

Figure 8. a-shows ultrasonic PWM vs: a- accuracy; b- power losses.
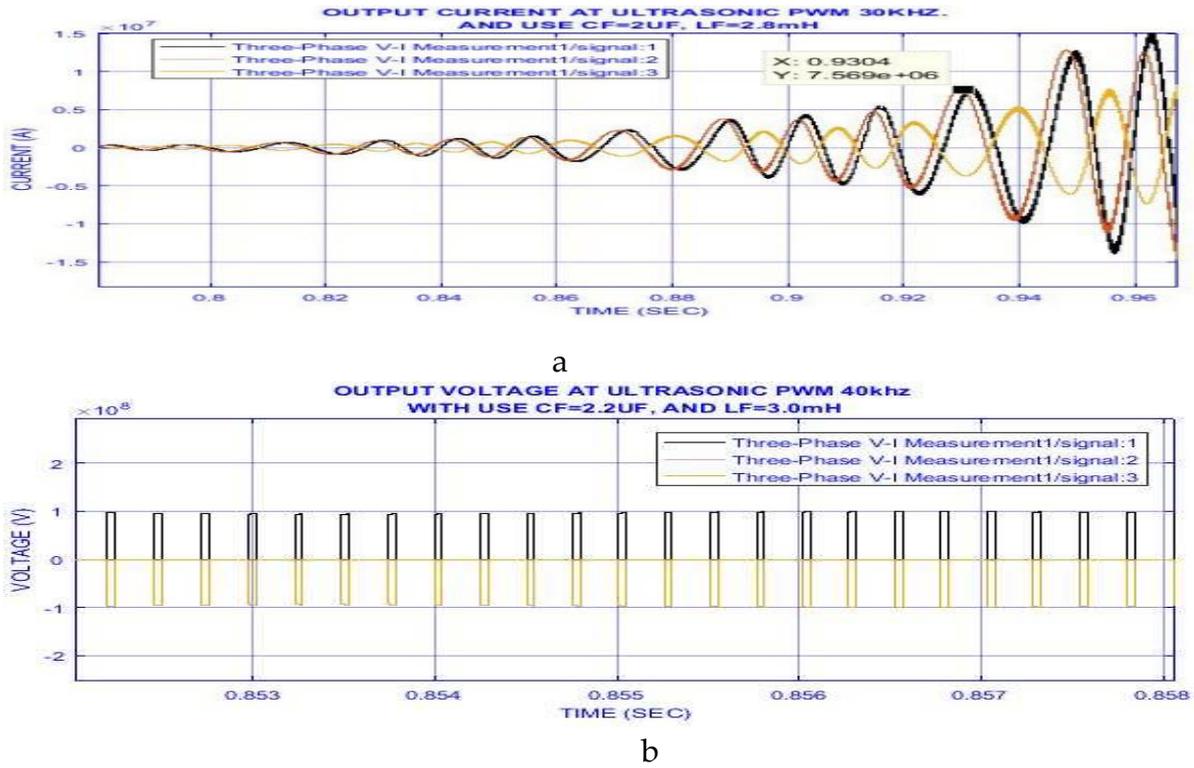
a

b

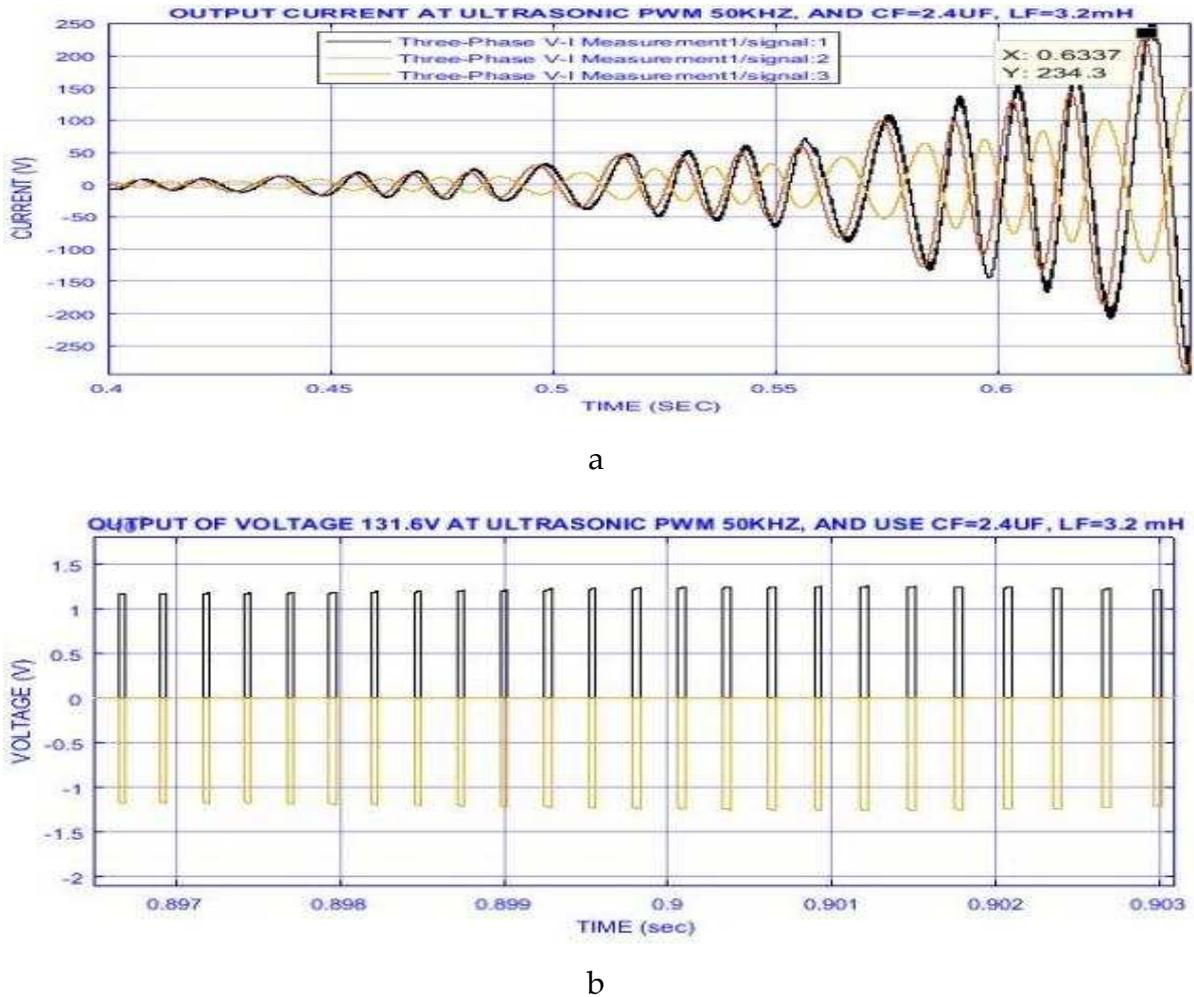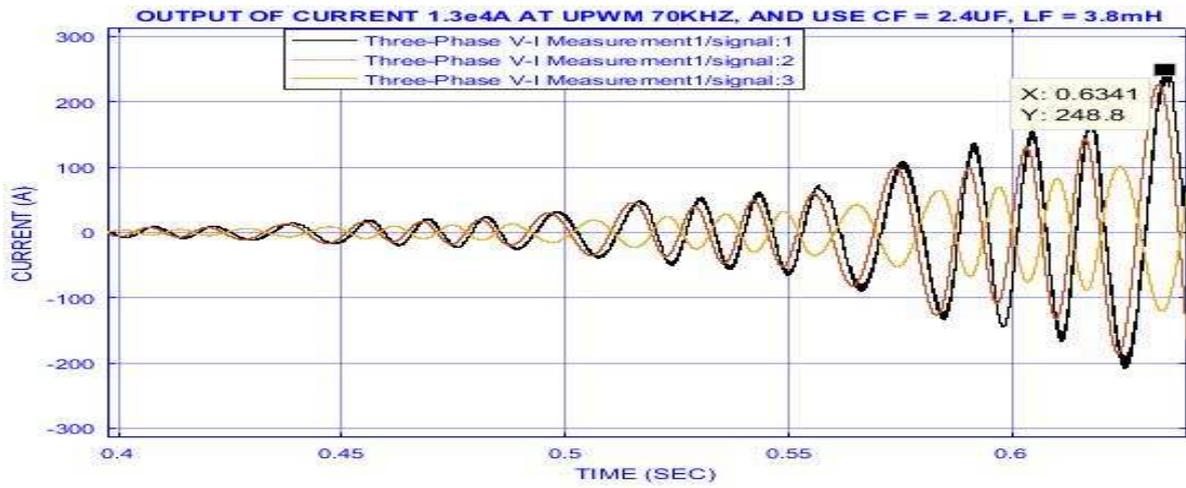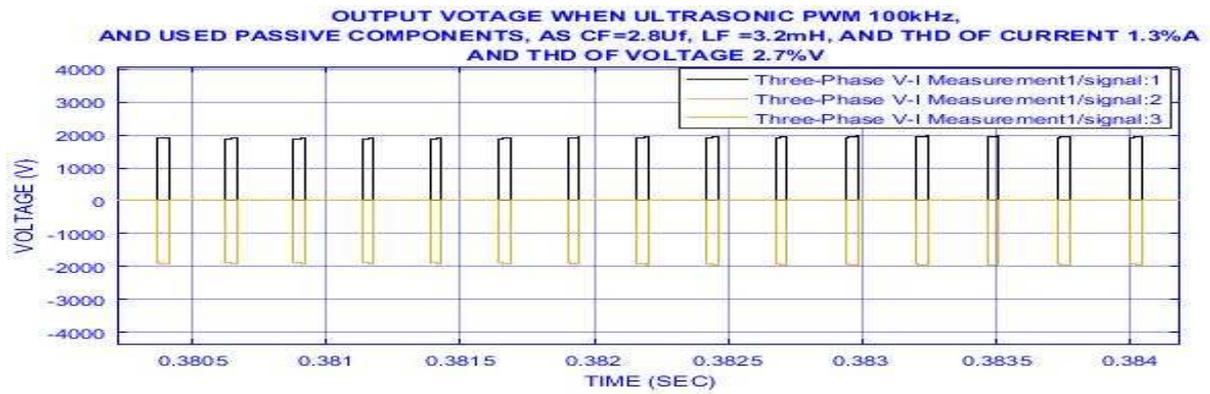**Figure 9.** Output when using UPWM of 30kHz; a- current, b- voltage when using UPWM of 40kH.

a

b

Figure 10. Shows the output at UPWM of 50kHz: a- current; b- voltage.

12

a
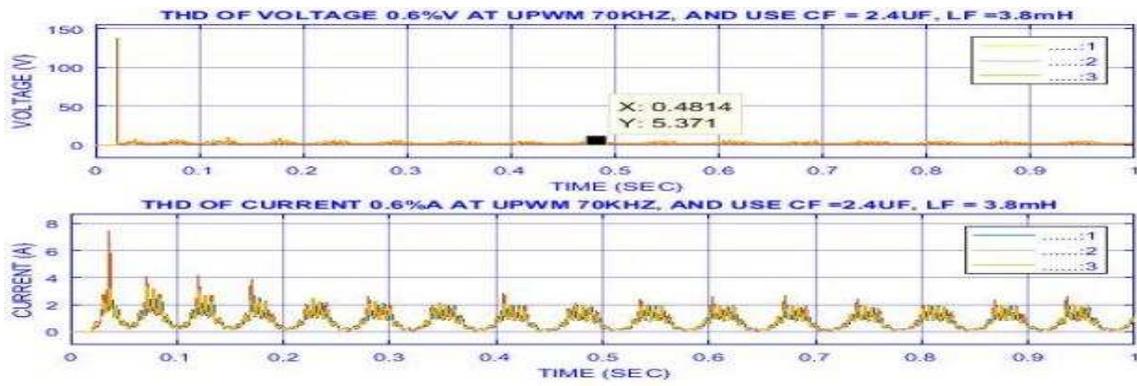
b

Figure 11. Shows of output at UPWM 70kHz: a- current b- THD is 0.6%.
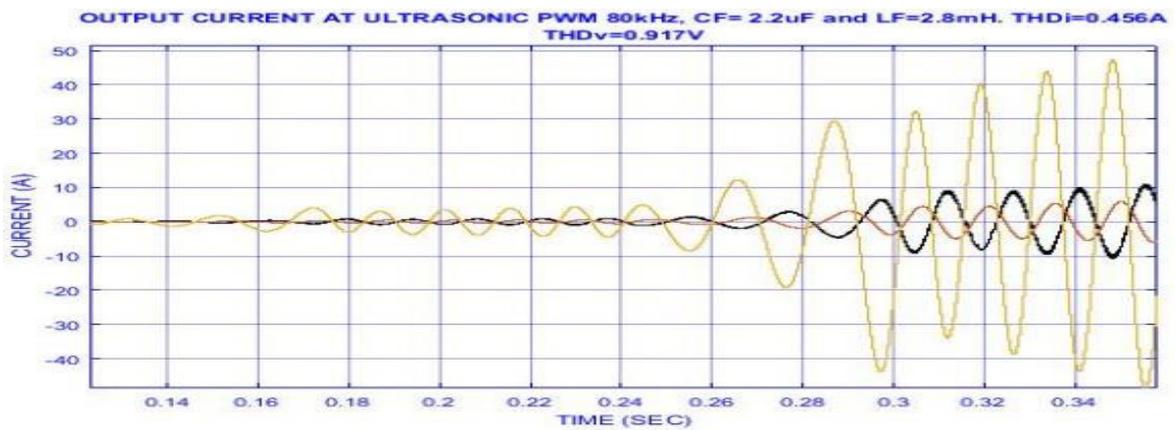
a
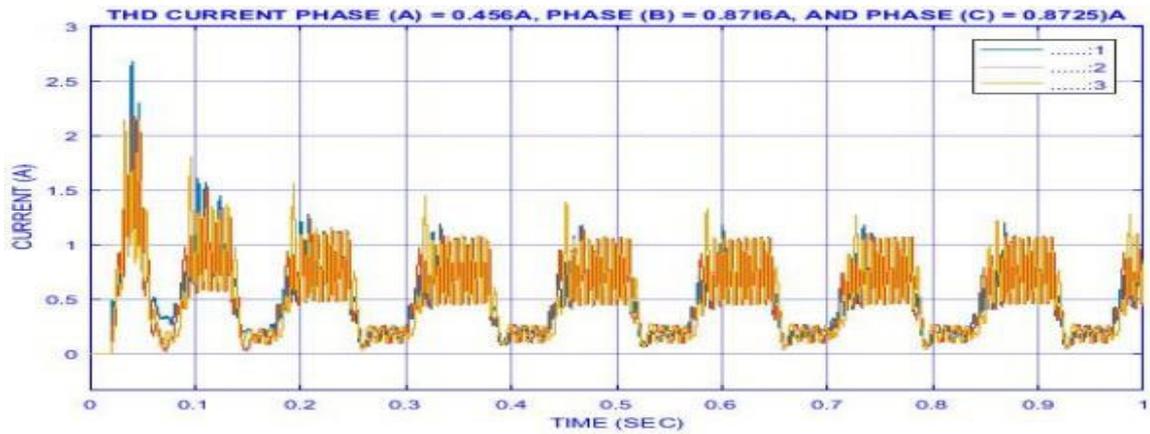
b

Figure 12. The output at UPWM is 80kHz; a- current. b- THD.
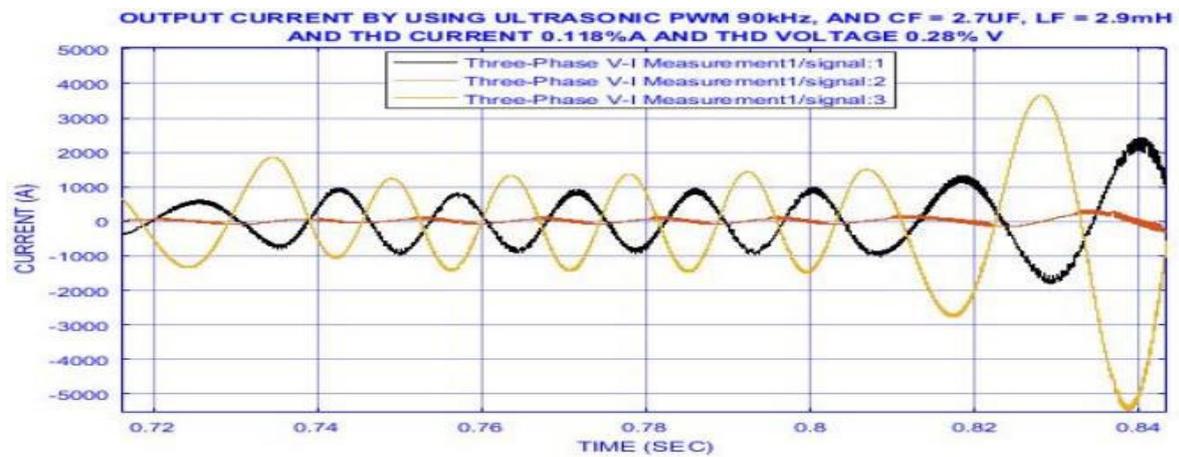
a
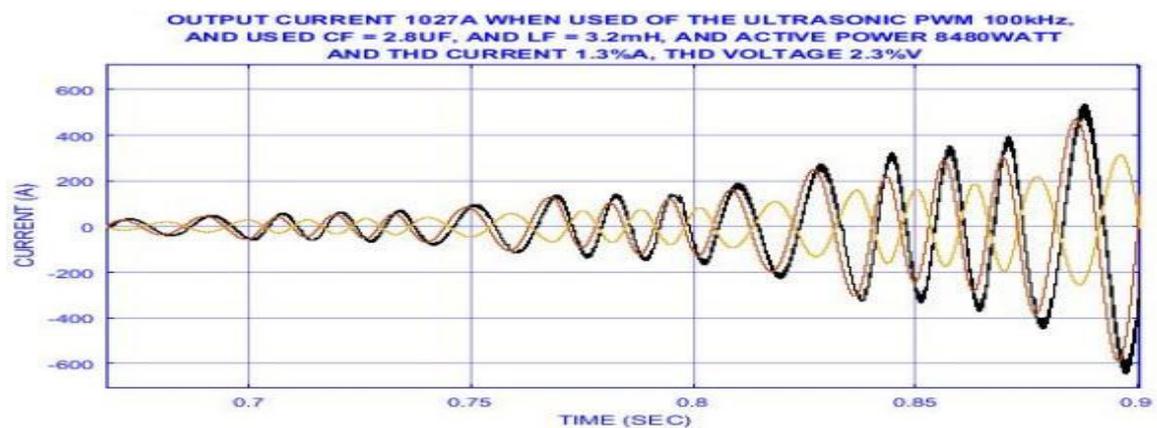
b

Figure 13. a- shows the output current with UPWM is 90kHz; b- shows the output current when using UPWM at 100kHz.

14

a

b
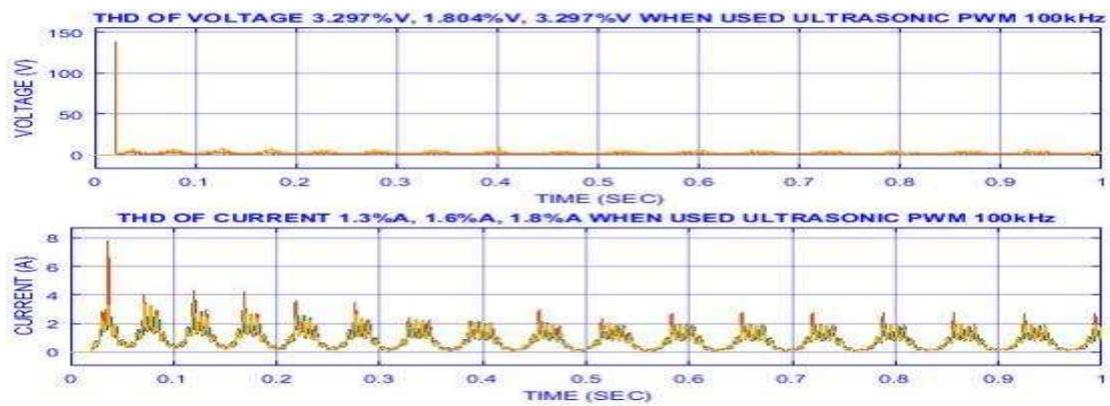
Figure 14. Output when using UPWM at 100kHz: a-voltage. b- THD.

a

15
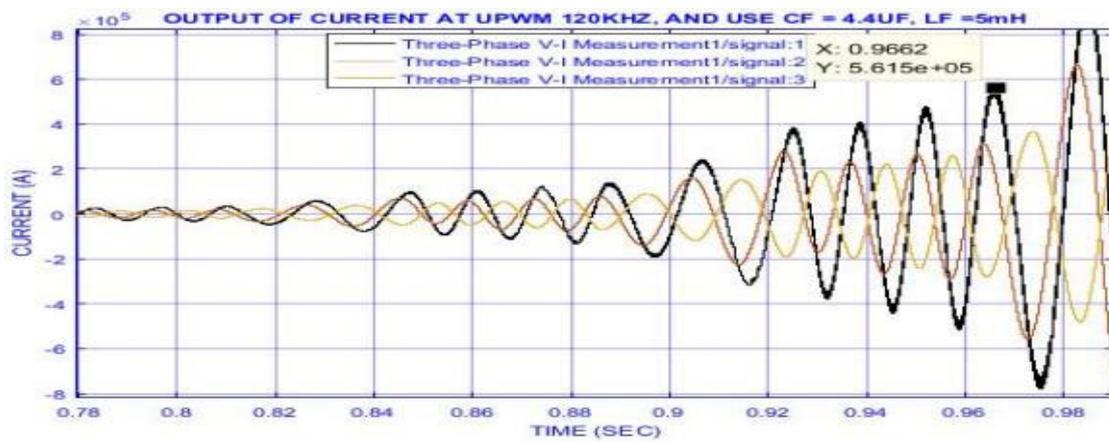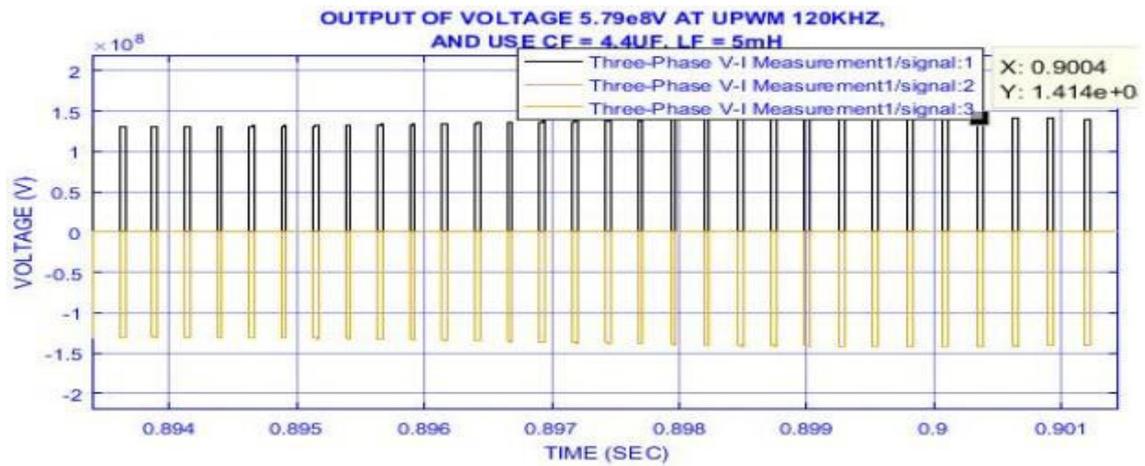
b

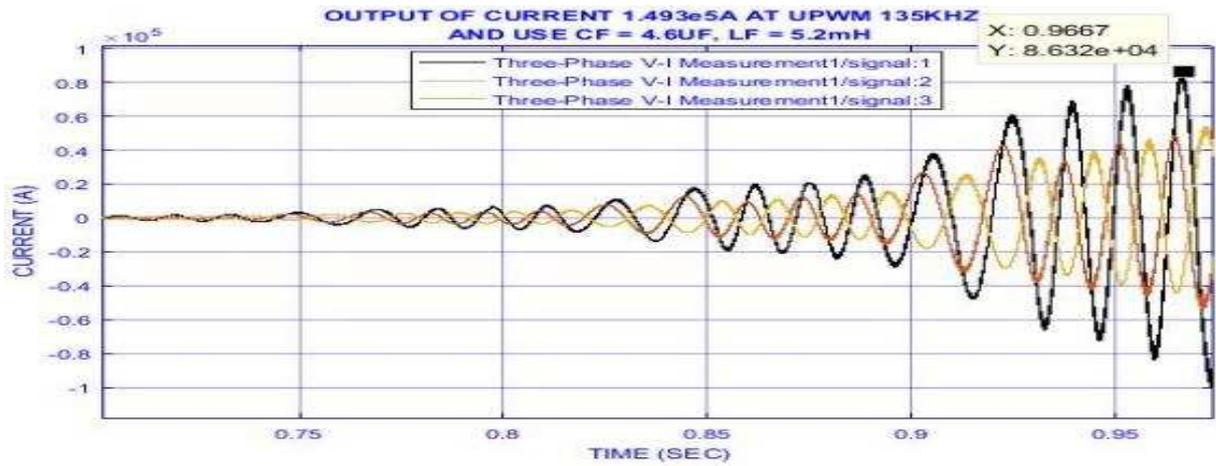**Figure 15.** The output when using UPWM is 120kHz, a-.current, b- voltage.
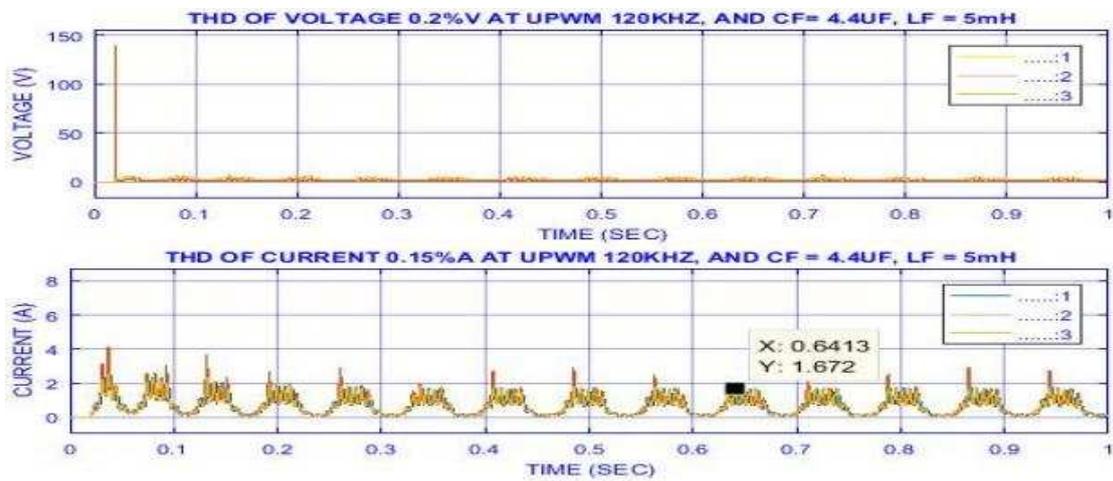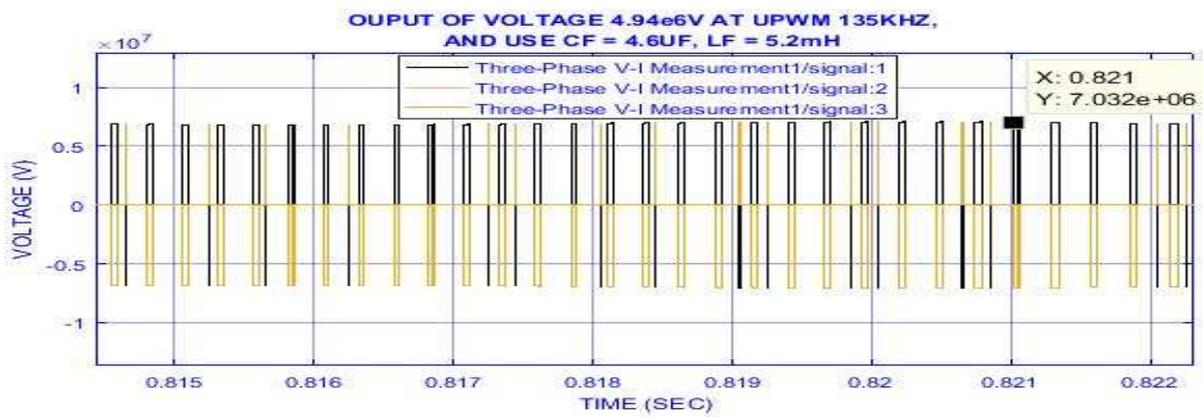

a
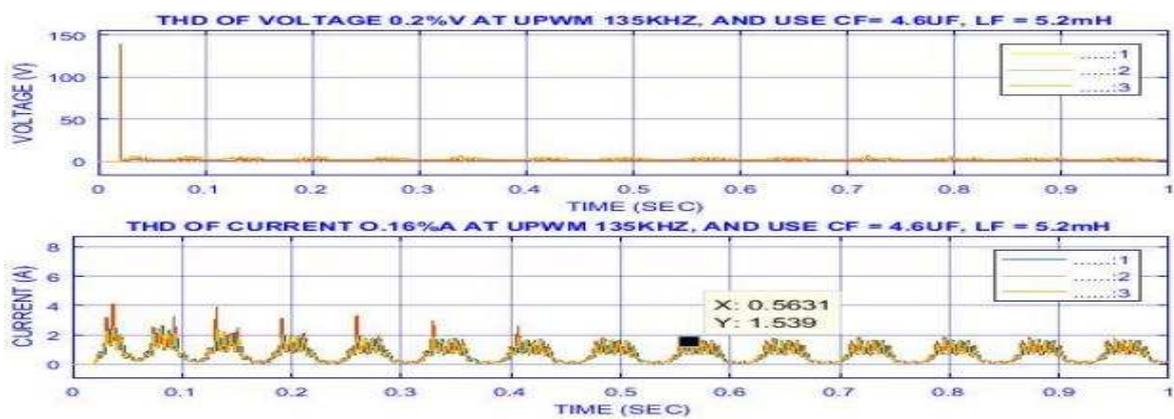
b

Figure 16. a- UPWM at 120kHz; a- THD is 0.1%; b- UPWM at 135kHz THD is 0.16%.
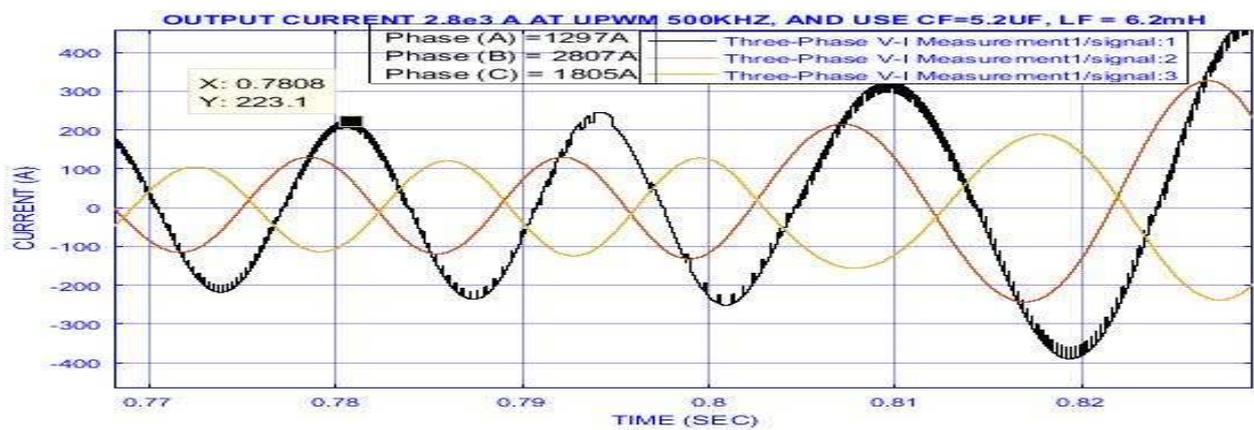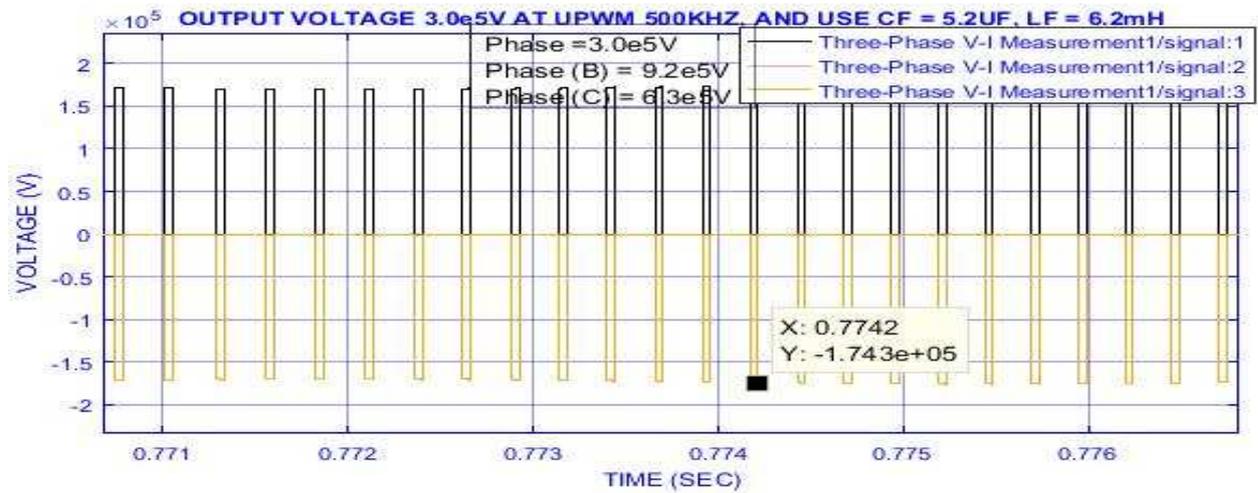
16

a

b

Figure 17. The output when using UPWM of 135kHz; a- current; b- voltage.

a

b

Figure 18. The output when using UPWM of 500 kHz; a- current; b- voltage.

4. Conclusion

That the use of ultrasonic PWM of the range at (20-500kHz) and enhancement to the action of these frequencies via FPGA, gave positive results with the presence of filter (CS) and with the use of the positive-phase sequence is a novelty, and the obtaining high accuracy in the inverter, and significantly reducing losses in the output. as well the oscillator circuit with 4GHz was used as accuracy control of all parameters of the inverter by software only and so not needed external components to control the output and by that the inverter became of low volume, and its cost is low. knowing that these frequencies gave response results to control the work of MOSFETs, In addition to the ADC design and its presence near the source of nutrition, it has DC link voltage synchronization, which led to the continuity of the work in the inverter. thus, the FPGA and ultrasonic PWM boost MOSFET work with high efficiency, knowing, that determination of the overvoltage and discharge in the inductance and DC link was by microcontroller (oscillator circuit with use 4GHz) to refinement ability of the MOSFETs to continuous work, as the results gave validate prove that.

References

1. S. J. Bale, P. D. Deshpande, M. Hough, S. J. Porter, and J. K. A. Everard, "High-Q Tuneable 10- GHz Bragg Resonator for Oscillator Applications," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 65, no. 2, pp. 281–291, 2018, doi: 10.1109/TUFFC.2017.2782567.
2. J. P. Caram, J. Galloway, and J. S. Kenney, "Voltage-Controlled Ring with FOM Improvement by Inductive Loading," *IEEE Microw. Wirel. Components Lett.*, vol. 29, no. 2, pp. 122–124, 2019, doi: 10.1109/LMWC.2019.2891168.
3. Y. Chen *et al.*, "A supply pushing reduction technique for LC oscillators based on ripple replication and cancellation," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 240–252, 2019, doi: 10.1109/JSSC.2018.2871195.
4. M. Yalsavar, Y. Salmanpour, M. Hajihosseini, and P. Karimaghaee, "Design and Manufacturing Modular Inverter with High Power and Frequency for Increasing Safety Factor in Industrial Applications," *2019 IEEE 5th Conf. Knowl. Based Eng. Innov. KBEI 2019*, pp. 526–530, 2019, doi: 10.1109/KBEI.2019.8735034.
5. R. Ebrahimi, N. Ayobi, P. S. Ghasemi, and E. N. Aghdam, "Real-Time Control of Resonance Point of Piezoelectric Transducers Based on Class D Power Converter," *ICEE 2019 - 27th Iran. Conf. Electr. Eng.*, pp. 336–340, 2019, doi: 10.1109/IranianCEE.2019.8786677.

6. K. U. Choi, T. D. Nguyen, S. G. Choi, and J. P. Hong, "High-Frequency Buffer- Feedback Oscillator with an RF Negative-Resistance Circuit," *IEEE Access*, vol. pp. 20964–20970, 2018, doi: 10.1109/ACCESS.2018.2818323.

7. E. Gutierrez, L. Hernandez, F. Cardes, and P. Rombouts, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures with Extended Noise Shaping," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 2, pp 444–457, 2018, doi: 10.1109/TCSI.2017.2737830.

8. J. C. Hertel, Y. Nour, and A. Knott, "Integrated Very-High-Frequency Switch Mode Power Supplies: Design Considerations," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 2, pp. 526–538, 2018, doi: 10.1109/JESTPE.2017.2777884.

9. L. Hernandez and E. Gutierrez, "Analytical evaluation of VCO-ADC quantization noise spectrum using pulse frequency modulation," *IEEE Signal Process. Lett.*, vol. 22, no. 2, pp. 249–253, 2015, doi: 10.1109/LSP.2014.2357071

10. G. La Tona, M. Luna, M. C. Di Piazza, M. Pucci, and A. Accetta, "Development of a high-performance, FPGA-based virtual anemometer for model-based MPPT of wind generators," *Electron.*, vol. 9, no. 1, 2020, doi: 10.3390/electronics9010083

11. T. Lei, N. Gong, L. Wang, Q. Q. Li, and H. W. Wang, "Design of the variable frequency oscillator in DC-DC converter," *Circuit World*, vol. 45, no. 2, pp. 80–85, 2019, doi: 10.1108/CW-01-2018-0003.

12. R. Makhoul *et al.*, "A Very High Frequency Self-Oscillating Inverter Based on a Novel Free-Running Oscillator," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8289–8292, 2019, doi: 10.1109/TPEL.2019.2904886.

13. K. M. Megawer, A. Elkholy, D. Coombs, M. G. Ahmed, A. Elmallah, and P. K. Hanumolu, "A 5GHz 370fsrms 6.5mW clock multiplier using a crystal-oscillator frequency quadruple in 65nm CMOS," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 61, pp. 392–394, 2018, doi: 10.1109/ISSCC.2018.8310349.

14. X. Meng, L. Zhou, F. Lin, and C. H. Heng, "A Low-Noise Digital-to-Frequency Converter Based on Injection-Locked Ring Oscillator and Rotated Phase Selection for Fractional-N Frequency Synthesis," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 27, no. 6, pp. 1378–1389, 2019, doi: 10.1109/TVLSI.2019.2898258.

15. Z. Rymarski, K. Bernacki, Ł. Dyga, and P. Davari, "Passivity-based control design methodology for UPS systems," *Energies*, vol. 12, no. 22, 2019, doi: 10.3390/en12224301.

16. M. Mohammadi, J. S. Moghani, and J. Milimonfared, "A Novel Dual Switching Frequency Modulation for Z-Source and Quasi-Z-Source Inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 5167–5176, 2018, doi: 10.1109/TIE.2017.2784346.

17. G. H. M. Tavares, M. L. G. Salmento, W. J. Paula, D. D. C. Pereira, and H. A. C. Braga, "Implementation of a high-frequency PWM signal in FPGA for GaN power devices switching," *14th Brazilian Power Electron. Conf. COBEP 2017*, vol. 2018-Janua, pp. 1–7, 2017, doi: 10.1109/COBEP.2017.8257309.