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Article

Analysis and Implementation of a Frequency Synthesis Based on Dual Phase-Locked Loops in Cs Beam Clock

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Abstract: The frequency synthesizer is a critical component in Cs beam clock technology. In this paper, we present a demonstration of a direct microwave frequency-synthesis chain for a cesium-beam atomic clock, which utilizes frequency multiplication and a dual-phase-locked loop mode. A detailed analysis of the frequency-synthesis chain is conducted, and a mathematical model is established. The phase settling time and system stability are simulated, measured, and verified. The experimental results for the phase settling time align with the simulation outcomes. The phase settling time can be adjusted within the range of 644.5 µs to 1.5 ms, and the absolute phase noise values are -63.7 dBc/Hz, -75.7 dBc/Hz, -107.1 dBc/Hz, and -122.5 dBc/Hz at 1 Hz, 10 Hz, 1 kHz, and 10 kHz offset frequencies, respectively. Additionally, the Ramsey fringes are detected, and the Allan deviations of the 10 MHz output from the cesium-beam atomic clock are measured to be 2.99×10^{-12} at 1s and 8.02×10^{-14} at 10,000 s.

Keywords: frequency synthesis; phase noise; phase settling time; stability analysis

1. Introduction

Atomic clocks stabilize the frequency of an oscillator with high-frequency stability by aligning it to an atomic transition line[1–4]. Due to their exceptional frequency stability, atomic clocks are increasingly vital in various applications, including synchronization, precise timekeeping, information infrastructures, and fundamental physics research[5–10]. Cesium-beam clocks are widely used in these fields because of their advantages, such as good long-term frequency stability, compact structure, low power consumption, and ease of operation[11–14]. The frequency-synthesis chain, a crucial component of cesium-beam clocks, generates a highly pure microwave signal at 9.192 631 770 GHz to induce atomic magnetic resonance in a cesium-beam tube (CBT). The quality of the microwave signal directly influences the performance of the cesium-beam clock[15,16].

In recent decades, extensive research has been conducted to improve the frequency synthesis techniques used in cesium-beam clocks, focusing on enhancing stability, accuracy, and reliability. One research area has aimed at improving the stability and accuracy of the frequency synthesis process by exploring techniques to reduce phase noise, spurious signals, and other sources of frequency instability[17–20]. Strategies include the use of noise reduction techniques, such as phase-locked loops (PLLs) and digital signal processing algorithms, to enhance the precision and stability of the generated frequencies[21,22]. Additionally, efforts have been made to enhance the long-term stability of cesium-beam clocks[14,23]. This involves studying the aging characteristics of frequency synthesis components and developing compensation methods to mitigate the effects of aging on frequency accuracy over extended periods. The Allan deviation, which measures the stability of an atomic clock, is particularly sensitive to the noise present in the local oscillator (LO) signal[24–26].

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Richard K. Karlquist, Leonard S. Cutler, and Robin P. Giffard observed that for slow modified modulation signals, adjustments in frequency and amplitude steps are necessary to accurately investigate the central and adjacent lobes of the principal Ramsey lines. Achieving optimal time utilization of the measurement requires accurate settling of the microwave signal phase within 1.5 ms. Once the frequency and amplitude are settled, the individual steps only take an additional 3 ms to complete, maximizing time utilization[15,16]. Currently, no literature analyzing the phase settling time of the frequency-synthesis chain has been found.

This paper presents the development of a microwave frequency-synthesis chain, based on frequency multiplication and dual-phase-locked loop circuits, that converts a 10 MHz reference clock to a 9.192 631 770 GHz output for a cesium-beam atomic clock. The phase settling time of the microwave frequency-synthesis chain is evaluated through theoretical analysis and simulation of the dual-PLL system. The phase settling time can be reduced by appropriately adjusting the gain of the PLL. By continuously adjusting the loop filter gain of the PLL, the measured phase settling times range between 644.5 us and 1.5 ms. Optimizing the system parameters allows for improved frequency stability.

2. Schematic and Experimental Setup og the Frequency-Synthesis Chain

Figure 1 presents the block diagram of the frequency-synthesis chain, which utilizes a dual-PLL circuit. The primary purpose is to function as a dual-loop jitter cleaner (dual-loop mode) when a reference clock with accurate frequency is employed to generate an output clock with ultra-low jitter. The dual-loop mode helps maintain a high phase-detector frequency and loop bandwidth in the clock generation PLL, especially when the greatest common divisor of the reference clock frequency and the output clock frequency is small. This approach prevents a low phase-detector frequency and minimizes the output phase noise of the clock.

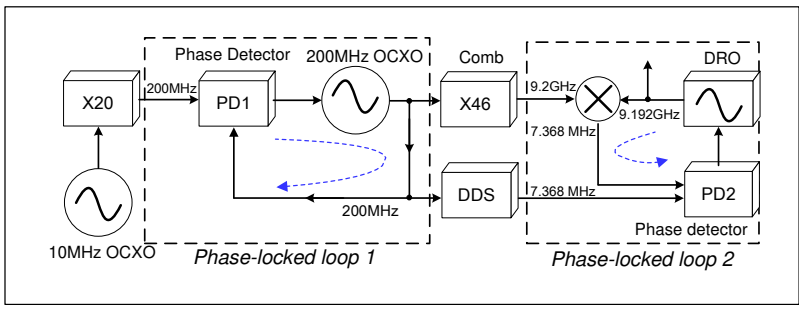

Figure 1. Basic architecture of the frequency-synthesis chain.

In Figure 1, a 20× frequency multiplier is used to multiply the 10 MHz reference clock to 200 MHz. Then, the 200 MHz clock is phase-detected with the clock output from the 200 MHz Oven-controlled crystal oscillators (OCXO) in the first phase detector (PD1) at a frequency of 200 MHz. The output signal from the 200 MHz OCXO drives a frequency comb generator to produce harmonics of 200 MHz. In the second PLL (PLL2), the 46th harmonic of 200 MHz is selected by a narrow-band bandpass filter, and then the 9.2 GHz is mixed in the second phase detector (PD2) with another 9.192 GHz produced by the dielectric resonant oscillator (DRO). By a direct digital synthesis (DDS) module, a 7.368 MHz signal is generated. Then, the 7.368 MHz and the 9.192 GHz are compared in PD2. When the two PLLs are both phase-locked, a precise frequency at 9.192 631 770 GHz is ready. Considering the frequency precision error of 10 MHz reference, the final output signal will have a certain frequency deviation.

Figure 2 illustrates a more detailed architecture diagram of the frequency-synthesis chain, consisting of four main parts. Part (1) involves a 10 MHz OCXO source with ultralow phase noise. In Part (2), a 200 MHz clock from the 20× frequency multiplier is filtered and amplified before being compared with the 200 MHz OCXO output clock in PD1. The phase error signal generated by PD1 is filtered and then fed back to the proportional–integral controller to drive the 200 MHz OCXO. The

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signal from the 200 MHz OCXO output is split into two paths using a coupler. In the first path, the output clock is amplified with a low-noise amplifier, filtered, and sent to PLL2 as the reference clock. In the other path, the 200 MHz clock is amplified, filtered, and used to drive a comb generator. The 46th harmonic of the comb generator's output is band-pass filtered, amplified with a microwave amplifier in part (3), and then sent to the mixer in part (4). In PLL1, a splitter is used to generate two 200 MHz signals, with one of them serving as the sampling rate of the direct digital synthesis (DDS, AD9854) to generate a 7.368 230 MHz clock[27]. In part (4), the 9.2 GHz microwave generated by the comb generator is mixed with the 9.192 GHz microwave generated from the DRO, and the resultant signal is passed through a power splitter. This process generates a 7.368 230 MHz clock. The two 7.368 230 MHz clocks are compared with each other to produce a phase error signal[28,29]. The phase error signal is then low-pass filtered, conditioned by the PID2, and used to drive the DRO[23]. When the frequency-synthesis chain is in a phase-locked state, the 9.192 GHz microwave is directed to an amplitude control module to excite atomic transitions in the CBT.

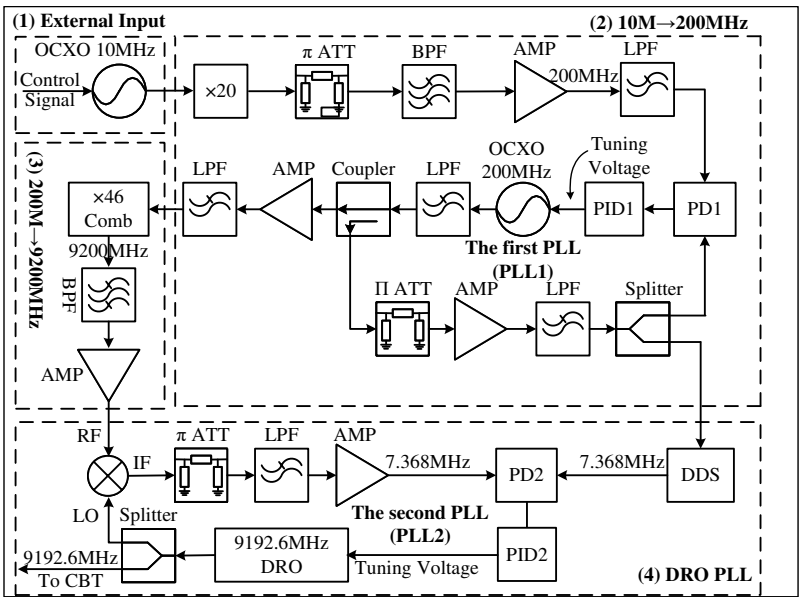

Figure 2. The experimental setup of the frequency-synthesis chain. Part (1): 10 MHz OCXO. Part (2): the First PLL, including 20× frequency multiplier. Part (3): 200 MHz to 9.2 GHz. Part (4): the Second PLL, including the DRO. AMP, amplifier; ATT, attenuator; PD, phase detector; PID, proportional–integral–derivative controller; LPF, low-pass filter; BPF; band-pass filter.

The phase noise of the output in the loop bandwidth of a PLL is primarily caused by the input reference clock, following the deterioration according to the 20 × log N rule. Outside of this bandwidth, the phase noise performance is mainly determined by the internal voltage-controlled oscillator (VCO) of the PLL. In Figure 2, PLL1 employs a narrow-loop bandwidth of 150 Hz to preserve the frequency accuracy of the reference signal while suppressing noise from higher offset frequencies. The 200 MHz OCXO has an output power of approximately +10 dBm, a tuning sensitivity of around 50 Hz/V, and a voltage tuning range of 0V to 8V. Similarly, the DRO operates at an output power of approximately +15 dBm, a tuning sensitivity of about 2.2 MHz/V, and a voltage tuning range of 0V to 9V. It is important to note that all input and output signals are matched to 50 Ω impedance.

Given the limitations in frequency accuracy of the 10 MHz reference clock, it is essential for the final microwave signal to be precisely adjustable within a range of approximately ±1 kHz, with a high frequency resolution of less than 0.1 Hz. To achieve this level of precision, the DDS module assumes a critical role within the frequency synthesis chain. In this structure, the DDS module is integrated to generate a 7.368 MHz clock with a remarkable frequency resolution of up to 0.7 μHz[23,28]. Accurate frequency matching holds significant importance in the design of highly stable atomic clocks[30,31].

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3. Theoretical Analysis and Simulation of the Frequency-Synthesis Chain

3.1. Analysis of the model for the PLLs

From control theory, the PLL phase-transfer function H(s) can be defined, which establishes a relationship between the input reference clock and the output of the PLL. Figure 3 depicts a simplified configuration based on the architecture of the frequency-synthesis chain shown in Figure 2. In an analog PLL circuit, the mixer primarily functions as a phase detector.

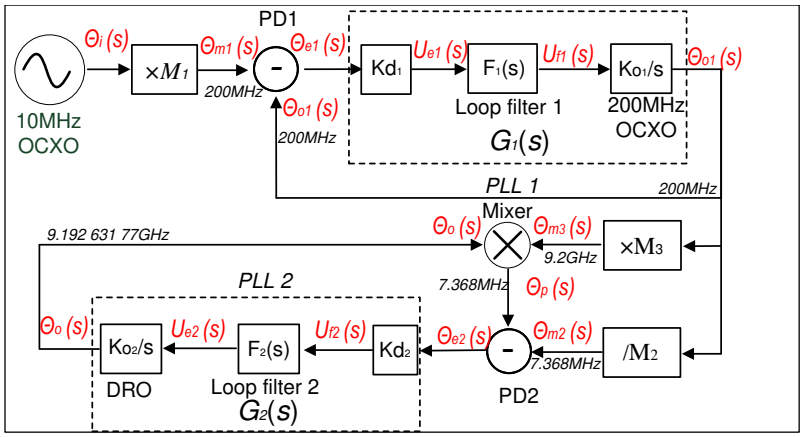

Figure 3. Simplified configuration of the frequency-synthesis chain.

In PLL1, as illustrated in Figure 3, the 10 MHz reference clock undergoes direct multiplication by a factor of M_1 to obtain a 200 MHz clock through the use of two cascaded frequency multipliers. The resulting clock is then compared with the 200 MHz clock generated from the 200 MHz OCXO in PD1. Thus, the phase argument of the 200 MHz clock $\Theta_{m1}(s)$ is given by

$$\Theta_{m1}(s) = M_1\Theta_i(s), \tag{1}$$

where $\Theta_i(s)$ represents the phase argument of the 10 MHz reference clock. $U_{e1}(s)$ is defined as the phase error signal generated by PD1. In the complex frequency domain, $U_{e1}(s)$ can be expressed as:

$$U_{e1}(s) = k_{d1}\Theta_{e1}(s) = k_{d1}(\Theta_{o1}(s) - \Theta_{m1}(s)), \tag{2}$$

where k_{d1} denotes the detector gain of PLL1. Θ_{e1} represents the phase argument of the error signal generated by PD1, while $\Theta_{o1}(s)$ is the phase argument of the 200 MHz OCXO output. Equation (2) presents a linearized model of PD1.

The output from the 200 MHz OCXO is divided into two paths by a coupler. The main path is utilized directly, while the other path is amplified, low-pass filtered, and further divided into two additional paths. One of these paths serves as the sampling rate of the DDS, while the other is fed back to PD1. In Figure 3, the transfer function of the first loop filter is defined as $F_1(s)$. Hence, the error signal of the filter can be expressed as

$$U_{f1}(s) = F_1(s)U_{e1}(s), \tag{3}$$

where $U_{f1}(s)$ represents the error signal from the first low-pass filter (LPF1) in PLL1, which is employed to tune the 200 MHz OCXO. In the complex frequency domain, the output signal from the 200 MHz OCXO is proportional to the control signal and can be given as

$$\Theta_{o1}(s) = \frac{k_{o1}}{s}U_{f1}(s), \tag{4}$$

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where k_{o1} represents the gain of the 200 MHz OCXO. When the phase error signal generated by PD1 is sufficiently small, the output signal from the mixer can be approximated by its argument. The transfer function $G_1(s)$ is defined as the first loop gain in Figure 3. Based on Eqs. (2)–(4), $G_1(s)$ can be expressed as

$$G_1(s) = \frac{\Theta_{o1}(s)}{\Theta_{e1}(s)} = \frac{k_{d1}k_{o1}F_1(s)}{s}, \tag{5}$$

Furthermore, $H_1(s)$ in Figure 3 relates the input 10 MHz reference clock to the 200 MHz OCXO output. $H_1(s)$ can be expressed as

$$H_1(s) = \frac{\Theta_{o1}(s)}{\Theta_{i1}(s)} = \frac{\Theta_{o1}(s)}{\Theta_{e1}(s)/M_1} = \frac{k_{d1}k_{o1}M_1F_1(s)}{s + k_{d1}k_{o1}F_1(s)}, \tag{6}$$

Equations (5) and (6) represent the mathematical model of PLL1. Assuming PLL1 is phase-locked in the time domain, the 200 MHz output signal u_{o1} can be expressed as

$$u_{o1}(t) = a_1 cos(\omega_1 t + \theta_{o1}), \tag{7}$$

where a_1 represents the amplitude argument of the signal, and ω_1 and θ_{o1} are the radian frequency and initial phase of the 200 MHz OCXO output, respectively.

Figure 3 illustrates the utilization of the 200 MHz clock to drive a comb generator, generating harmonics of 200 MHz. We denote the order of these harmonics as M_3, and the M_3 order of the 200 MHz harmonic as $u_{m3}(t)$. Simultaneously, another 200 MHz clock serves as a sampling clock for the DDS (AD9854) to produce a 7.378 23 MHz clock. We denote the division factor of the DDS module as M_2, and the signal derived from the DDS module as $u_{m2}(t)$. The calculations for these two signals are as follows

$$u_{m2}(t) = a_{m2} cos\left(\frac{1}{M_2}\omega_1 t + \frac{1}{M_2}\theta_{o1}\right) \tag{8}$$

$$u_{m3}(t) = a_{m3} cos(M_3\omega_1 t + M_3\theta_{o1}), \tag{9}$$

where a_{m2} and a_{m3} represent the amplitude arguments of the respective signals.

In PLL2, the center frequency of the dielectric resonant oscillator (DRO) is denoted as ω_{m2}, and $u_0(t)$ represents the output signal of the DRO. For our design, the center frequency ω_{m2} is approximately 9.192 GHz. In the time domain, $u_0(t)$ is given by the equation

$$u_0(t) = a_0 cos(\omega_2 t + \theta_0), \tag{10}$$

where a_0 represents the amplitude and θ_0 is the initial phase of the DRO. The signal ω_2 is mixed with the 9.2 GHz signal from the comb generator to generate a clock at 7.368 MHz. This 7.368 MHz clock is then compared with the 7.378 MHz signal generated from the DDS. We define the output signal generated by the mixer as $u_p(t)$

$$u_p(t) = \frac{a_0 a_{m3}}{2} cos\left[(\omega_2 + M_3\omega_1)t + (\varphi_0 + M_3\theta_{o1})\right] + \frac{a_0 a_{m3}}{2} cos\left[(\omega_2 - M_3\omega_1)t + (\varphi_0 - M_3\theta_{o1})\right], \tag{11}$$

Equation (11) describes $u_p(t)$ as having two parts. The first part is a higher-frequency signal, which is eliminated by a low-pass filter (LPF). The latter part represents a 7.368 MHz signal, which is compared with the 7.378 MHz signal from the DDS in PD2. The phase argument of the error signal generated by PD2 is denoted as $\theta_{e2}(s)$. In the complex frequency domain, based on Eqs. (7)-(11), the phase error signal $\theta_{e2}(s)$ of PD2 can be expressed as

$$\theta_{e2}(s) = \theta_0(s) - \left(M + \frac{a_0 a_{m3}}{2}\right) cos\left[(\omega_2 - M_3\omega_1)t + (\varphi_0 - M_3\theta_{o1})\right], \tag{12}$$

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where $\theta_0(s)$ represents the phase argument of the DRO output. The transfer function $G_2(s)$ is defined as the loop gain of PLL2 shown in Figure 3. Thus, the phase argument of the DRO output $\Theta_0(s)$ can be expressed as

$$\begin{aligned}\Theta_o(s) &= \frac{k_{o2}}{s}U_{f2}(s)\\ &= \frac{k_{o2}}{s}F_2(s)k_{d2}\Theta_{e2}(s)\\ &= \frac{k_{o2}}{s}F_2(s)k_{d2}\left[\Theta_o(s) - \left(M_3 + \frac{1}{M_2}\right)\Theta_{o1}(s)\right],\end{aligned} \tag{13}$$

In Equation (13), k_{d2} represents the detector gain of the DRO, k_{o2} is the DRO gain, and $F_2(s)$ is the transfer function of the second loop filter in PLL2. Consequently, the phase-closed loop transfer function $F_2(s)$ of PLL2 can be derived as

$$H_2(s) = \frac{\Theta_o(s)}{\Theta_{o1}(s)}, \tag{14}$$

Based on the aforementioned analysis, the phase-closed loop transfer function of the microwave frequency-synthesis chain $H(s)$ can be expressed as

$$\begin{aligned}H(s) &= H_1(s)H_2(s)\\ &= \frac{k_{d1}k_{d2}k_{o1}k_{o2}M_1M_2M_3F_1(s)F_2(s) + k_{d1}k_{d2}k_{o1}k_{o2}M_1F_1(s)F_2(s)}{M_2s^2 + M_2\left[k_{d1}k_{o1}F_1(s) + k_{d2}k_{o2}F_2(s)\right]s + M_2k_{d1}k_{d2}k_{o1}k_{o2}F_1(s)F_2(s)},\end{aligned} \tag{15}$$

In Figure 4, an active loop filter is utilized, with a transfer function gain of $k_p(1/T_i + 1)$, where k_p and T_i represent the gain and integration time of the loop filter, respectively. In this paper, a first-order passive LPF is employed, and its transfer function can be expressed as $L(s) = 1/(\tau s + 1)$, where τ denotes the time delay of the LPF. For our design, only the proportional gain is utilized in the proportional-integral (PI) regulator, as shown in Figure 2. Consequently, $k_p(1/T_i + 1)$ can be simplified to k_p. Additionally, the transfer function mode of an active loop filter can be expressed as $F(s) = k_p/(\tau s + 1)$. Therefore, we have

$$F_1(s) = k_{p1}/(\tau_1 s + 1), \tag{16}$$

$$F_2(s) = k_{p2}/(\tau_2 s + 1), \tag{17}$$

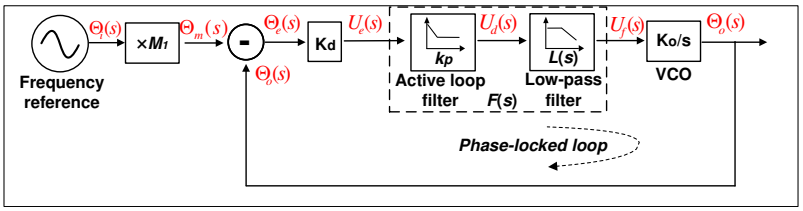

Figure 4. Functional block diagram of the active loop filter PLL.

3.2. *Simulation results*

3.2.1. Transient analysis

The PLL ensures the phase alignment of the output clock with the reference clock. Although the phase of the reference clock can experience instantaneous distortion, the PLL requires a certain amount of time to adjust its phase. Thus, the phase settling time plays a crucial role in evaluating the frequency-synthesis chain[32].Simulations of $H(s)$ using Eq. (15) were conducted based on the theory

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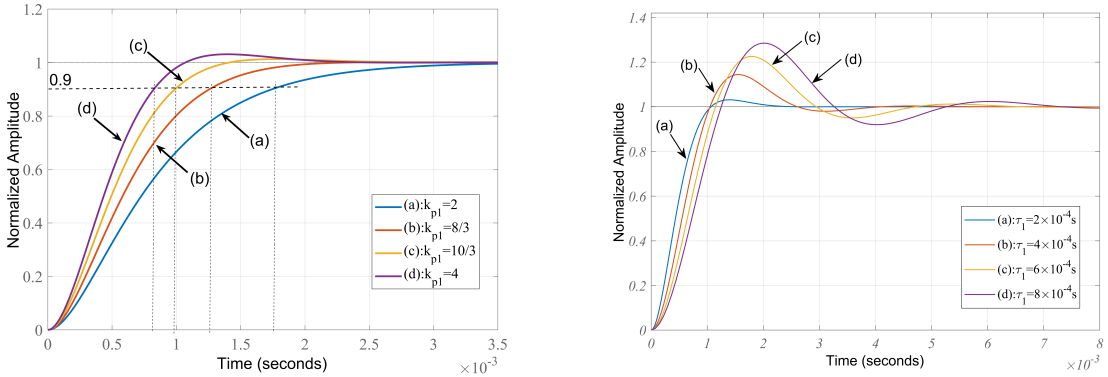
presented in Section 2. The parameter values used are as follows: $M_1 = 20$, $M_2 = 200/7.368230$, $M_3 = 46$, $k_{d1} = 1$ V/rad, $k_{d2} = 1$ V/rad, $k_{o1} = 90$ Hz/V, and $k_{o1} = 2.2$ MHz/V. Since the frequency-synthesis chain consists of two PLLs, the parameters k_p and τ can be adjusted for both PLLs.

Assuming that the parameters k_{p2} and τ_2 are fixed simplifies the calculation of the modulation signal gain applied in the frequency-synthesis chain. The given parameter values were substituted into Eq. (15), and the step responses of the system are depicted in Figure 5. Figure 5(a) illustrates the settling times of the phase step response for various values of k_{p1} (ranging from 2 to 4 in steps of 2/3), while τ_1 remains fixed at 2×10^{-4} s. The settling times obtained are 1.52 ms, 1.07 ms, 822 µs, and 674 µs,respectively. For comparison, Figure 5(b) demonstrates the effect of varying τ_1 (ranging from 2×10^{-4} s to 8×10^{-4} s) while k_{p1} remains fixed at 2.



(a) (b)

Figure 5. Simulation results showing the phase step response. (a) Parameter τ_1 was fixed, while parameter k_{p1} was varied. (b) Parameter k_{p1} was fixed, while parameter τ_1 was varied.

The simulation results indicate that increasing k_{p1} leads to a decrease in the settling time of the signal. Conversely, keeping k_{p1} constant and increasing τ_1 results in an increase in both overshoot and settling time of the signal. Therefore, reducing τ_1 not only shortens the transient response duration but also suppresses phase fluctuations. However, reducing τ_1 widens the bandwidth of the active loop filter, which introduces more noise. Hence, for practical design purposes, the loop filter gain k_{p1} should be appropriately increased while τ_1 is appropriately decreased.

Figure 6 demonstrates that varying parameter k_{p2} has minimal effect on the settling time. Thus, the settling time of the frequency-synthesis chain is primarily determined by PLL1.

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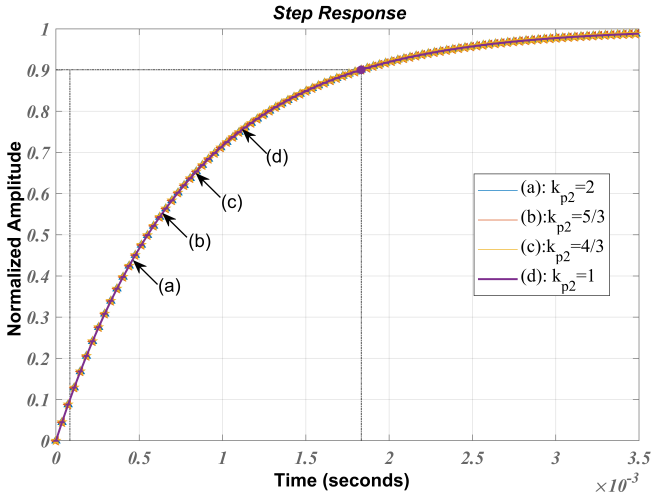
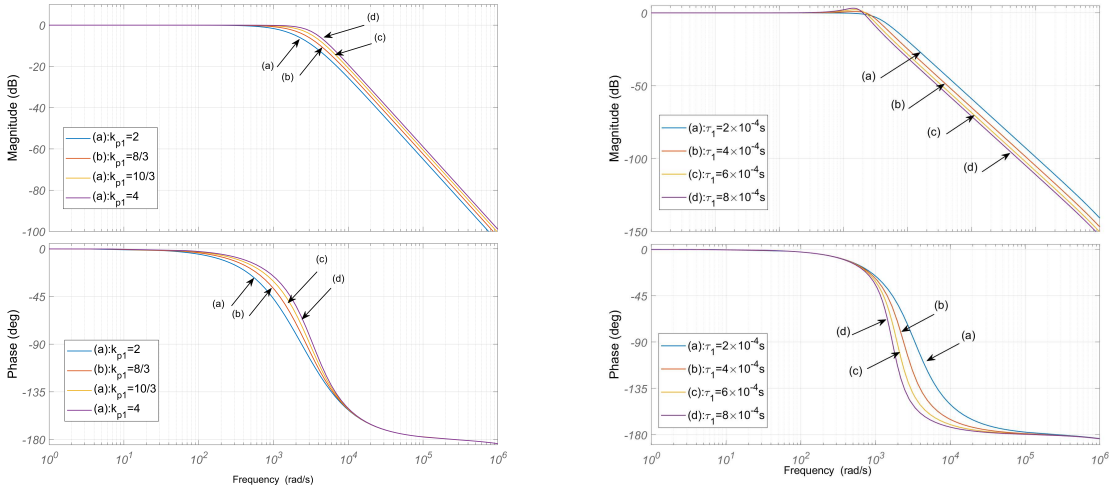


Figure 6. Simulation results showing the phase step response. Parameter τ_2 was fixed, and parameter k_{p2} was varied.

3.2.2. Stability analysis

The impact of the loop filtering parameters of PLL1 on the transient characteristics and system stability is evident from the analysis in Section 3. Bode plots illustrating the frequency domain with the application of an external modulation signal are presented in Figure 7.



(a) (b)

Figure 7. Bode diagrams: (a) $\tau_1 = 2 \times 10^{-4}$ s and k_{p1} from 2 to 4 and (b) $k_{p1} = 4$ and τ_1 from 2×10^{-4} s to 4×10^{-4} s.

Figure 7(a) indicates that, when the τ_1 parameter is fixed, increasing the loop filter gain k_{p1} leads to an increase in gain margin, phase margin, and stability. Conversely, Figure 7(b) demonstrates that, when the k_{p1} parameter is fixed, an increase in τ_1 results in a decrease in gain margin, phase margin, and stability. System stability is maintained when the modulation frequency is below 150 Hz (equivalent to $150 \times 2\pi$ rad/s), as the phase deviation between the stepping signal and the reference clock remains close to zero. However, when the modulation frequency exceeds 150 Hz, the phase gain starts to decrease. As the modulation frequency increases, the phase gain decays rapidly, leading

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to reduced system stability. Based on the simulation results, the following guidelines for setting parameters k_{p1} and τ_1 are recommended:

(1) Moderately increasing k_{p1} optimizes settling time.

(2) Parameter τ_1 should be adjusted in combination with parameter k_{o1}. Appropriate reduction of parameter τ_1 enhances settling time and effectively suppresses overshoot.

4. Experimental Results and Verification

4.1. Settling time measurement

In Section 2.2, the configuration of the phase-setting measurement was simplified to a functional block, as depicted in Figure 8. A dual-channel arbitrary function generator (AFG; Tektronix AFG3022B) was employed as the phase shifter, as shown in Figure 4. Figure 8 illustrates that the arbitrary waveform generator (AWG) utilizes the 10 MHz OCXO as a reference to generate two identical 10 MHz signals, which are then used to drive the two frequency synthesizers (FSs) for generating two cesium atomic resonant frequencies at 9.192 631 770 GHz. One of the FSs proposed in this paper is denoted as FSA, while the other is a commercial microwave signal synthesizer (FSB; SMB100A, Rohde & Schwarz).

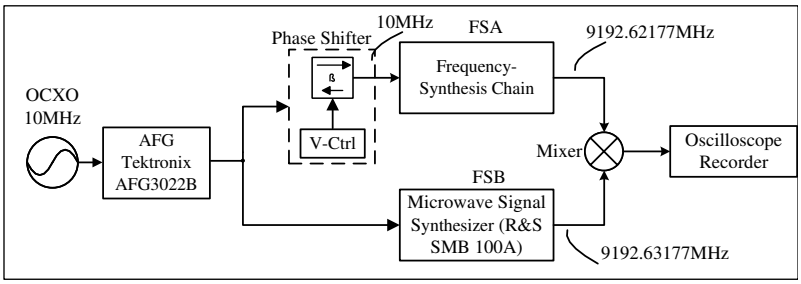

Figure 8. Simplified configuration for measuring the phase-settling ability.

The 10 MHz signal generated by the AWG can be phase-modulated to simulate the phase step function, allowing the FSs to experience a phase step by utilizing the phase shift produced by the AWG. Phase modulation is applied to FSA to generate the phase step, while maintaining a fixed phase in FSB. Since the two 9.192 GHz signals are simultaneously phase-locked to the same 10 MHz reference clock, their phases are precisely synchronized. The two signals are compared in a mixer (Mini-circuits, ZMX-10G+), and the resulting phase error signal is recorded using a digital storage oscilloscope. In accordance with the mixer principle described in Section 3.1, the higher-frequency output from the mixer is eliminated due to the bandwidth limitation of the oscilloscope, while the lower-frequency component is retained. When the phase step signal is applied to FSA, the mixer output signal is recorded, and the settling time of the step response is measured to assess the phase-tracking and phase-settling ability.

When the phase shift signal is applied to the 10 MHz reference clock of FSA, the phase response affecting the frequency of 9.192 631 770 GHz is multiplied by 919.2. Consequently, the minimum phase shift of the AWG is 0.01°, resulting in an approximate 9.192° phase shift at 9.192 631 770 GHz. The remarkable property of the DDS in an FS, as per the DDS principle, is the agility of the phase shift. Therefore, in comparison to the phase shift time, the phase-settling time is insignificantly short and can be disregarded.

When FSA and FSB are simultaneously phase-locked to the same 10 MHz reference clock, as depicted in Figure 8, the output signal from the mixer becomes a direct current (DC) signal. We adjust the phase of FSA until the DC signal reaches its maximum negative value. The phase step is applied within the range of π, resulting in an approximate phase shift of 0.2° applied to the 10 MHz reference. The measured values are compared with the simulation results under the same conditions, as shown in Figure 9. The dotted lines represent the simulation results, while the solid lines depict the results obtained using the configuration described in Figure 8.

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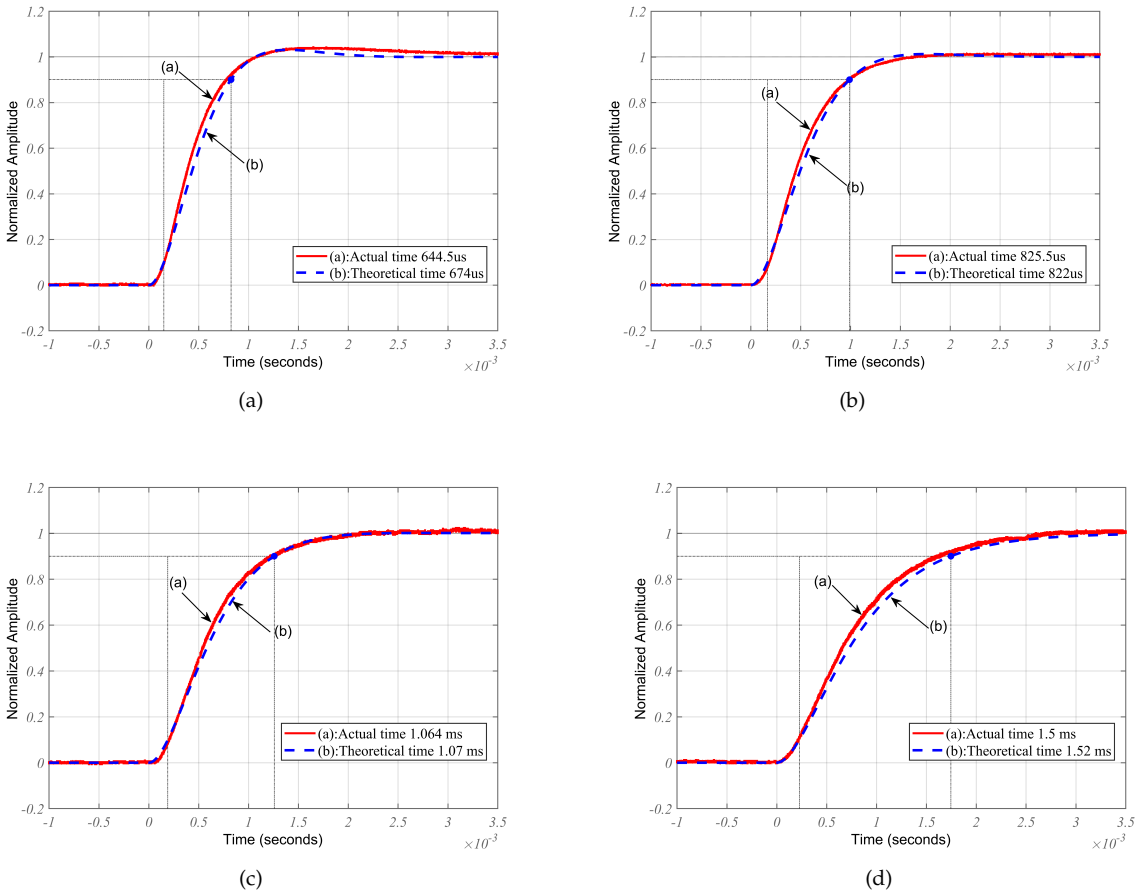

Figure 9. Phase step response. Dotted lines are the theoretical simulation results and the solid lines are the actual measurements.

Figure 9 illustrates the phase step response for various values of the loop filter gain $F_1(s)$. As the $F_1(s)$ parameter increases from 2 to 4 in steps of 2/3, the measured settling times are 1.5 ms, 1.064 ms, 825.5 µs, and 644.5 µs, respectively. The measured results align with the simulated results, providing evidence that the theoretical calculation for the transfer function of the synthesis and the experimental setup for measuring the phase step response are accurate and reasonable.

4.2. Phase noise measurement

Figure 10 presents the absolute phase noise measurements for a frequency synthesis chain consisting of a 10 MHz reference clock, 200 MHz OCXO, and DRO. The phase noise measurements were conducted using the R&S FSWP26. The 10 MHz reference clock is sourced from an OXCO. As discussed in Section 3, PLL1 and PLL2 were set with bandwidths of 150 Hz and 300 kHz, respectively. Figure 10(a) illustrates the absolute phase noises of the 10 MHz reference clock, which are measured at -123.8 dBc/Hz, -137.5 dBc/Hz, -158.5 dBc/Hz, and -165.5 dBc/Hz at 1 Hz, 10 Hz, 1 kHz, and 10 kHz offset frequencies, respectively. The output clock of the 200 MHz OCXO in its free-running state was measured at a power level of approximately +26 dBm, using a signal passed through a directional coupler and amplifier. The absolute phase noises at 1 Hz, 10 Hz, 1 kHz, and 10 kHz offsets were recorded as -56.5 dBc/Hz, -93.2 dBc/Hz, -145.3 dBc/Hz, and -163.6 dBc/Hz, respectively (see Figure 10(c)). While PLL1 is locked, the absolute phase noises of the 200 MHz OCXO signal are observed to be -97.5 dBc/Hz, -110.1 dBc/Hz, -145.0 dBc/Hz, and -163.8 dBc/Hz at 1 Hz, 10 Hz, 1 kHz, and 10 kHz offset frequencies, respectively (see Figure 10(b)). Comparing Figure 10(c) and Figure 10(b), it is evident that the phase noise performance exhibits an improvement of approximately 40 dB around

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the 1 Hz offset frequency at a carrier frequency of 200 MHz. In PLL1, a narrow-loop bandwidth of around 150 Hz is employed to suppress higher offset frequency phase noise while ensuring low phase-noise performance for PLL2. As a result, PLL2 can operate with a moderate loop bandwidth of 300 kHz.

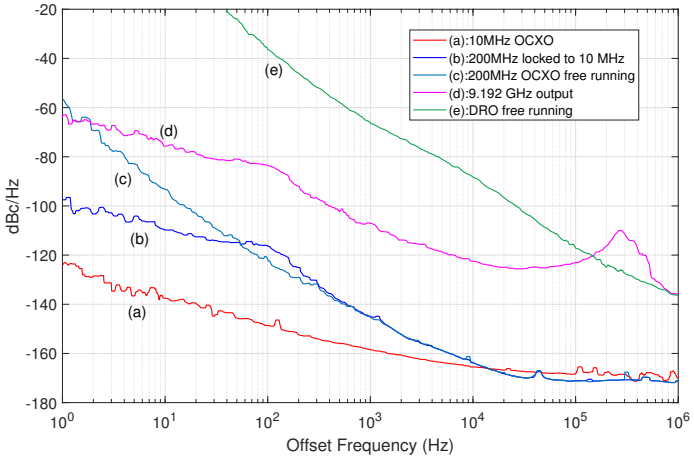

Figure 10. Absolute phase noise plots. (a) 10 MHz OCXO, (b) 200 MHz phase-locked to 10 MHz, (c) 200 MHz OCXO free running, (d) 9.192 GHz phase-locked to 10 MHz, (e) free-running DRO.

The selection of the loop bandwidth for PLL2 aims to leverage the superior high-offset frequency phase-noise characteristics of the DRO and the favorable low-offset frequency phase noise of the 200 MHz OCXO. Figure 10(d) illustrates the phase noises at 9.192 GHz when the frequency synthesis chain is locked, which are measured as -63.7 dBc/Hz, -75.7 dBc/Hz, -107.1 dBc/Hz, and -122.5 dBc/Hz at 1 Hz, 10 Hz, 1 kHz, and 10 kHz offset frequencies, respectively. When the DRO operates in a free-running state, as depicted in Figure 10(e), the phase noises are recorded as -66.2 dBc/Hz and -88.3 dBc/Hz at 1 kHz and 10 kHz offsets, respectively. Notably, it can be observed from Figure 10(e) that the phase noises at 1 Hz and 10 Hz offsets and a carrier frequency of 9.192 GHz are only 0.8 dB and 2.5 dB worse than the 20 logN rule derived from the 10 MHz reference clock. Consequently, the frequency synthesis chain demonstrates favorable phase noise performance at low offset frequencies below 150 Hz.

In Figure 10(d), the phase noise plot exhibits two inflection points around the offset frequencies corresponding to the two loop bandwidths. By appropriately increasing the loop bandwidths of both PLLs, a significant improvement in the phase noise performance can be achieved for offset frequencies lower than the bandwidths. However, a higher loop bandwidth results in more accumulated noise. Therefore, both loop bandwidths in the frequency-synthesis chain should be selected appropriately.

4.3. Frequency Stability measurement

The 9.2 GHz microwave signal was directed to the Ramsey cavity, where its resonant frequency was precisely tuned to match the clock frequency. Consequently, the separated oscillatory fields were successfully employed for hyperfine transition excitation in cesium. The interaction between the atomic beam and the microwave magnetic fields took place within the vacuum-sealed CBT, as illustrated in Figure 11(a). By scanning the microwave frequency emitted by the actual microwave source (Figure 11(b)), the Ramsey fringes were detected, as shown in Figure 11(c), thereby validating the design strategy of generating highly pure microwaves.

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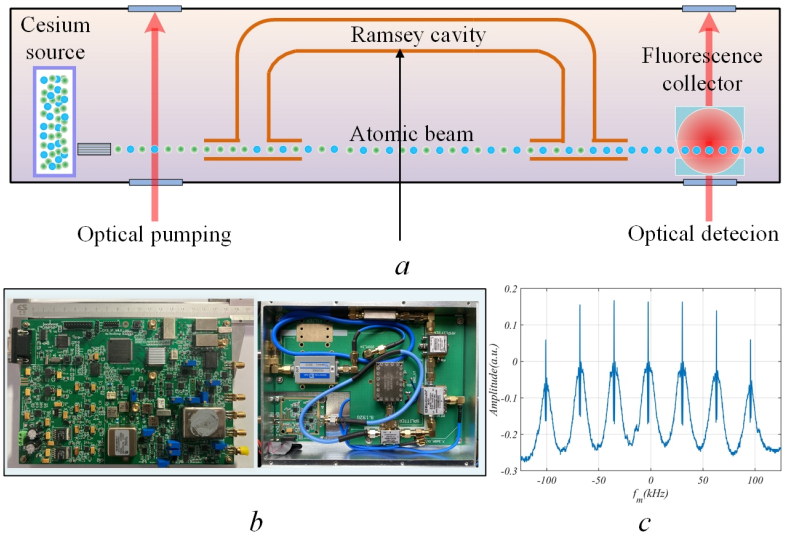

Figure 11. Ramsey fringes measurement. (a) Vacuum-sealed CBT. (b) Physical structure of the frequency-synthesis chain. (c) Ramsey fringes detected.

To characterize the long-term frequency stability, it is important to measure the Allan deviation of the device. We applied the frequency-synthesis chain to the cesium-beam atomic clock. In other words, the Allan deviation of 10 MHz output from the cesium-beam atomic clock was measured here. Figure 12 shows the Allan deviation over a period of 5 hours, measured by 3120A (Microsemi) at room temperature. It can be seen that the Allan deviations are 2.99×10^{-12} at 1s and 8.02×10^{-14} at 10,000 s.

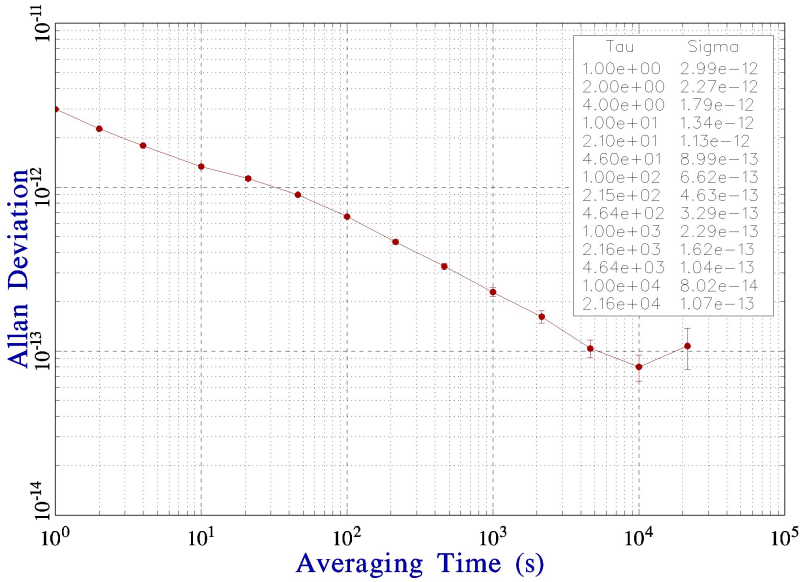

Figure 12. Allan deviation of the cesium-beam atomic clock using our frequency-synthesizer.

5. Conclusions

We constructed a high-performance microwave frequency synthesis chain using a dual-loop PLL architecture in the context of a cesium-beam atomic clock application. This architecture provides excellent phase noise performance and a suitable setup time. PLL1 is driven by an external 10 MHz reference clock, generating a precise and low-jitter 200 MHz frequency signal that acts as the reference driver clock for PLL2. We achieve ultra-low phase noise by allowing the OCXO to dominate the phase noise at low offsets, while the phase noise of the DRO remains dominant at high offsets. The absolute phase noise levels at 9.192 631 770 GHz were measured at -63.7, -75.7, -107.1, and -122.5 dBc/Hz at 1 Hz,

10 Hz, 1 kHz, and 10 kHz offset frequencies, respectively. Additionally, we established a mathematical model and conducted an analysis of the loop theory. Notably, we conducted a theoretical analysis of the phase settling time, which was then verified through simulations and found to be consistent with the actual measurements. The settling times can be adjusted within the range of 674 us to 1.52 ms. We validated the design strategy for generating highly pure microwaves by detecting the Ramsey fringes. Finally, we measured the Allan deviations of the 10 MHz output from the cesium-beam atomic clock, which yielded values of 2.99×10^{-12} at 1s and 8.02×10^{-14} at 10,000 s. Our research findings hold practical relevance for similar scenarios.

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