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Article

# Analysis of Turn-Off Losses in MOSFETs Equipped with the Kelvin Source

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**Abstract:** The paper first compares the turn-off performance of two package solutions (3-lead vs 4-lead) in Super-Junction MOSFETs. It is commonly assumed that the better performance (lower switching losses) of the 4-lead is obtained thanks to the decoupling of the power and driving loop. On the contrary, in this work, the experimental results, circuit models, and Kirchhoff laws have shown that the turn-off improvement (lower turn-off losses) obtained by adopting the Kelvin source is due to the lower inductance of the driver loop in comparison with the power loop inductance, instead of the decoupling between these loops.

**Keywords:** device modelling; MOSFET; packaging; parasitic inductance; switching losses

## 1. Introduction

Nowadays, in many applications, the market pushes towards the concurrent reduction of the bill of materials and the increment of power density [1,2]. The first target is achieved by adopting mature technologies with a good tradeoff between investment and performance [3]. The latter target can be obtained by operating the power converter at a high switching frequency to reduce the size of the passive components, thus also benefiting from the cost reduction [4]. However, an increment in the switching frequency inflicts increased switching losses that can considerably compromise power efficiency [5]. Furthermore, high-density high-frequency power converters lead to challenging thermal issues management [6]. This task becomes harder when the power converter is frequently operated at high/full load [7]. The thermal operating conditions of the power devices critically affect their lifetime [8].

Considering all the aforesaid aspects, a cost-effective solution can be reached using power devices able to ensure good efficiency when operated at high frequency and high load. SuperJunction (SJ) MOSFETs enhanced by the introduction of an additional source pin, called Kelvin source, is the best compromise solution [9]. At high loads, these devices presenting 4-lead (4L MOSFETs) strongly reduce the switching losses and, consequently, the device and converter operating temperature in comparison with 3-lead MOSFETs [10]. However, it is necessary to fully understand the reasons behind this improvement to fully exploits the advantages of 4L MOSFETs.

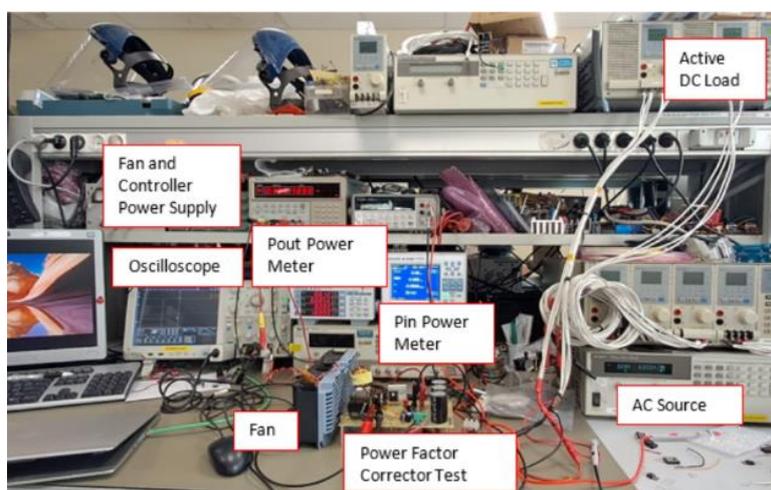
This paper investigates the improvement mechanisms involving a reduction of the switching losses during the turn-off [11]. Firstly, a comparison of the switching losses is presented. After that, the switching waveforms are analyzed to properly model the devices during the interval in which the greatest part of the turn-off losses occurs. Then, the circuit model is analyzed and an approximate analytical expression of the current slew rate is obtained for both kinds of devices packaging. The comparison of these equations has highlighted that the turn-off improvement obtained by adopting the Kelvin source is due to the lower inductance of the driver loop in comparison with the power loop inductance

## 2. Comparison of the experimental turn-off losses

A boost converter has been selected for analyzing the turn-off behaviour of 3L and 4L MOSFETs. The device is a TO-247-packaged N-channel MOSFET:

- breakdown voltage 650V;
- on-state resistance 37 m $\Omega$ ;
- maximum current 58 A.

The test vehicle is the boost converter reported in Figure 1 with the overall experimental setup.



**Figure 1.** Experimental setup.

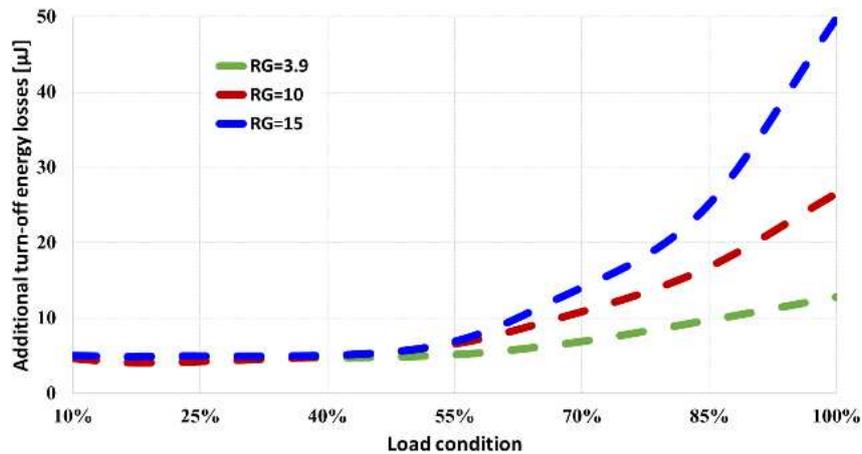
The test equipment consists of the following components.

- AC source: Agilent AC/DC power supply 6813B (1750VA).
- Oscilloscope: 1GHz Tektronix MS05140.
- Yokogawa power meter WT500 and WT310 to measure, respectively, the input and output power.
- Chroma DC Electronic Load Model 6314 to set the output current (active load).
- Tektronix current probe TCP0030 to measure the MOSFET current.
- Tektronix passive voltage probe (1:10) to measure the gate-source voltage.
- LeCroy passive voltage probe P6139B (1:100) to measure the drain-source voltage.

Finally, an auxiliary power supply has been used to supply the cooling fan.

Figure 2 reports the variation of the difference between the turn-off energy losses of 3L and 4L MOSFETs as a function of the converter load. In other words, the figure reports the additional switching losses due to the use of a 3L MOSFET instead of the same device enhanced by the Kelvin source.

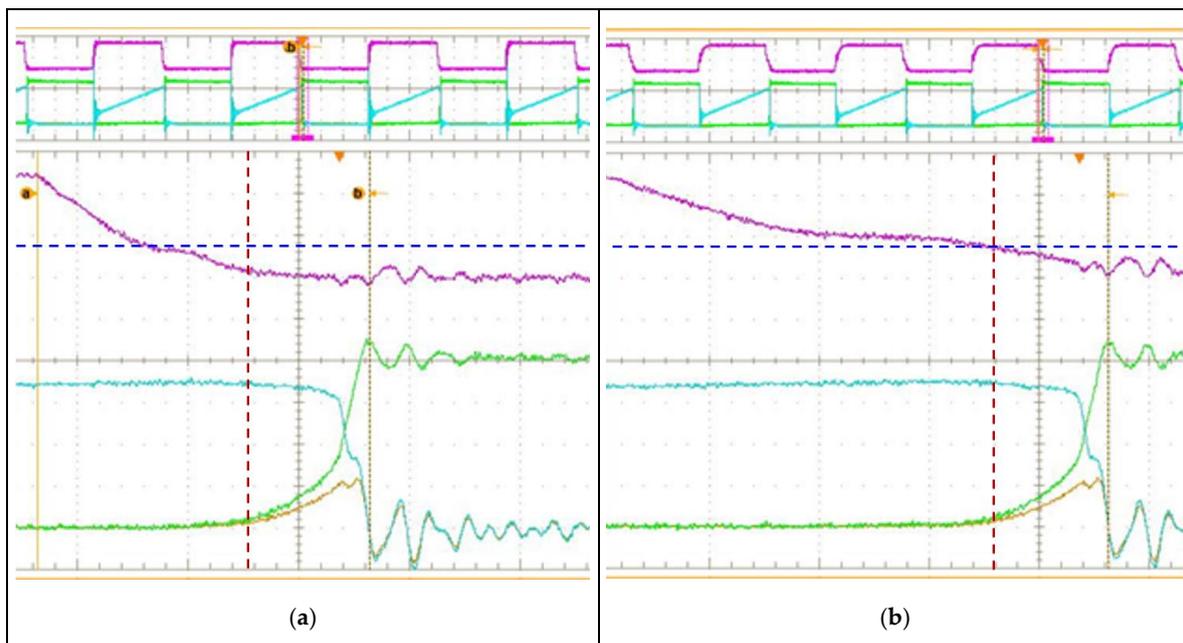
The results are reported for a typical  $R_G$  (3.9 $\Omega$ ) and greater values of the gate resistance. It is interesting to note that curves overlap for low load levels (<45%), this means that there is a negligible effect of the gate resistance. Moreover, also the load level has not any effect, as highlighted by the constant additional losses. For a load level greater than 45%, the curve does not overlap more. Consequently, the additional losses depend on the gate resistance: they increase as the resistance increases. Considering that the gate resistance regulates the switching speed that, in turn, affects the switching losses, the increment of the gate resistance slows more the 3L MOSFET turn-off than the 4L one.



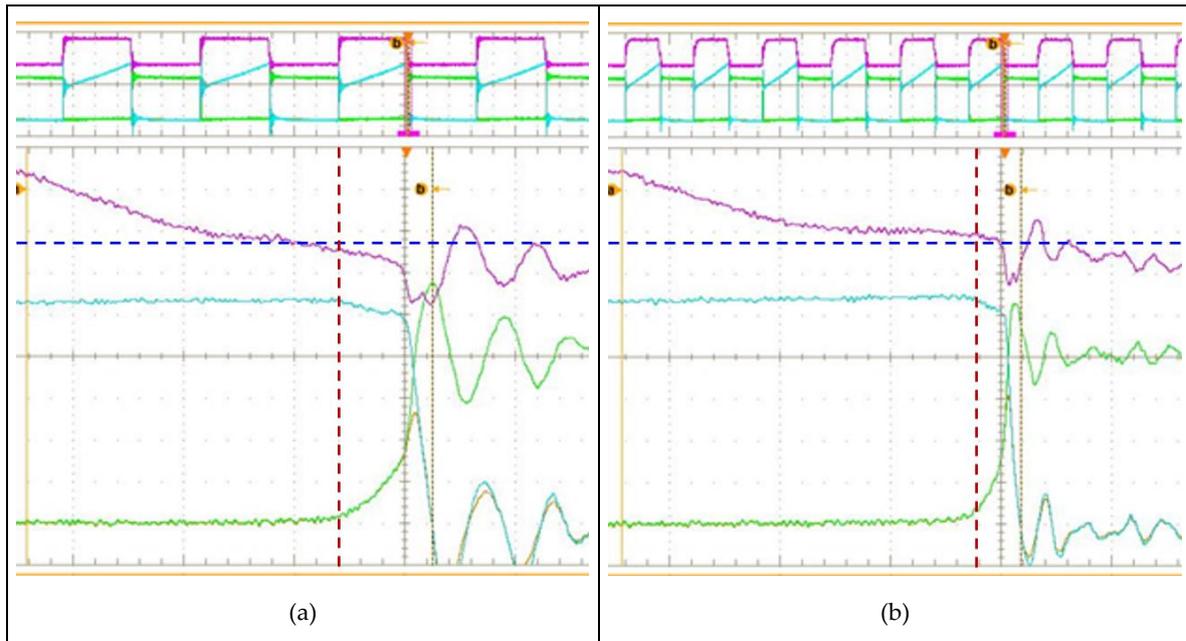
**Figure 2.** Difference between the turn-off energy losses of 3L and 4L MOSFET.

In this load range, also the load itself affects the additional energy losses because they increase as the load increases. Therefore, also the load current differently affects the turn-off switching speed.

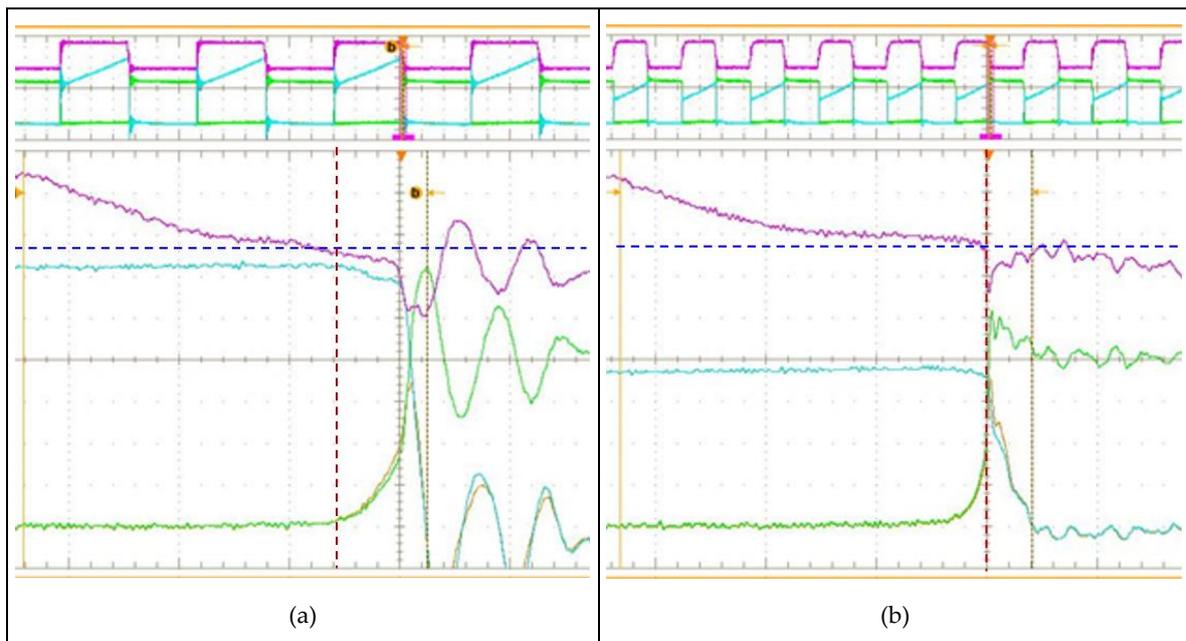
It is necessary to properly model the device during the turn-off in order to derive a formulation based on a circuit analysis aiming at understanding the effect of the gate resistance and load on the switching speed of 3L and 4L MOSFETs. The switching waveforms are analyzed with this aim. They are reported in Figures 3–8 for 3L (Figures 3–5) and 4L MOSFETs (Figures 6–8) considering a low load (Figure 3 and Figure 6), medium load (Figure 4 and Figure 7) and full load (Figure 5 and Figure 8) when the selected RG is, respectively, equal to  $3.9\Omega$  (a) and  $15\Omega$  (b).



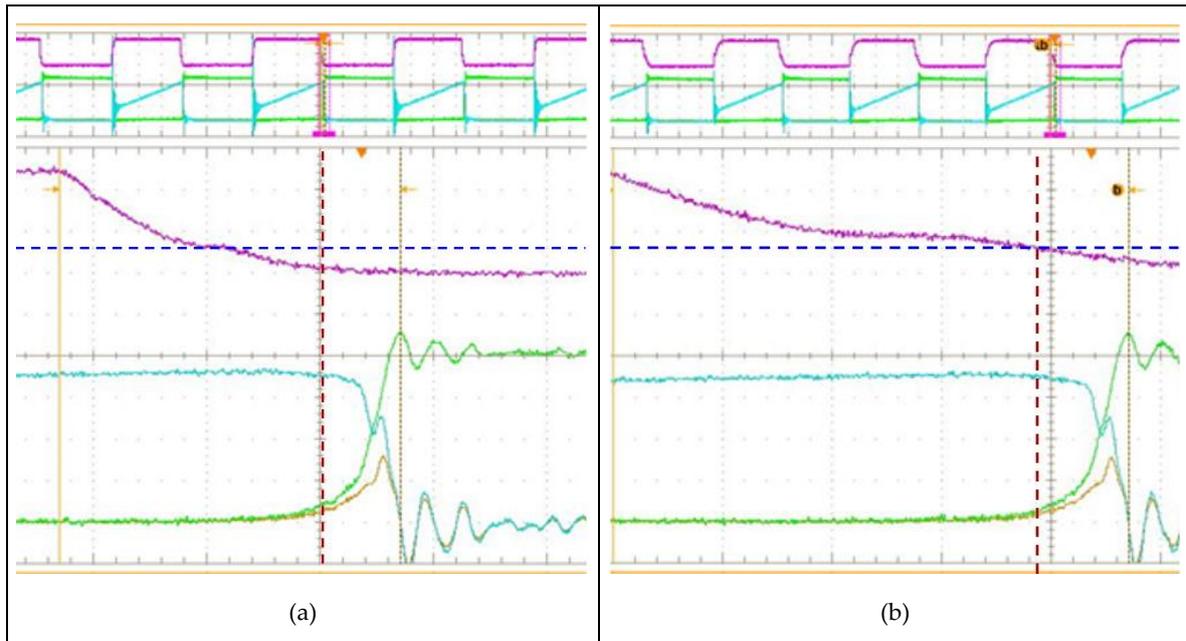
**Figure 3.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off of a 3L MOSFET at low load – (a)  $RG=3.9\Omega$  (b)  $RG=15\Omega$ .



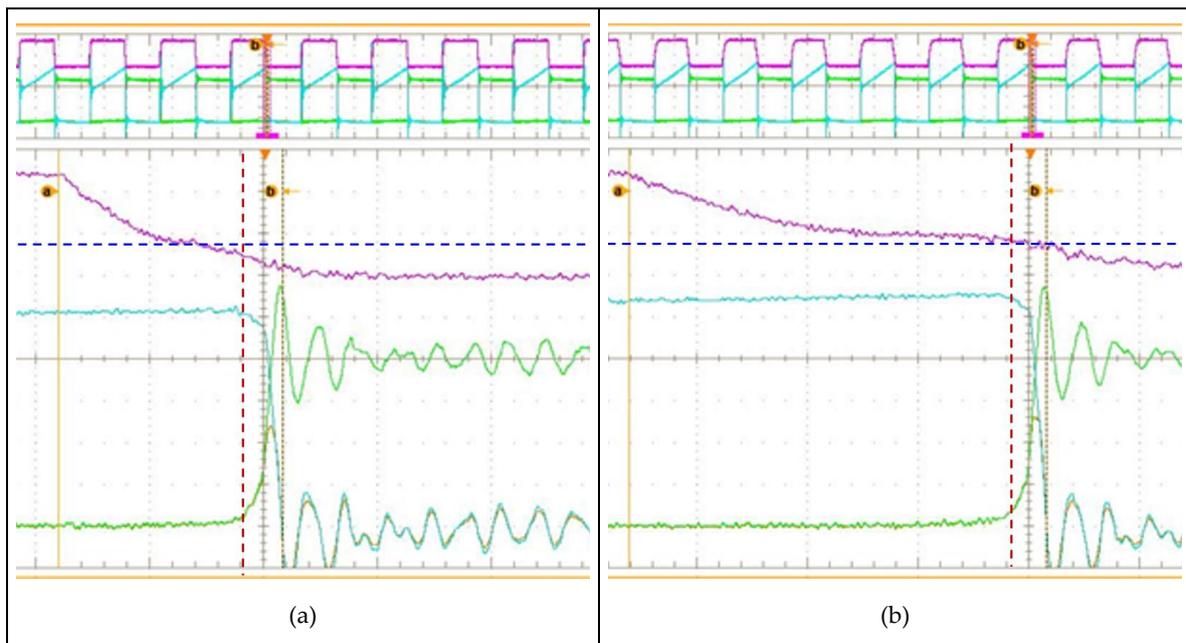
**Figure 4.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off of a 3L MOSFET at medium load – (a)  $R_G=3.9\Omega$  (b)  $R_G=15\Omega$ .



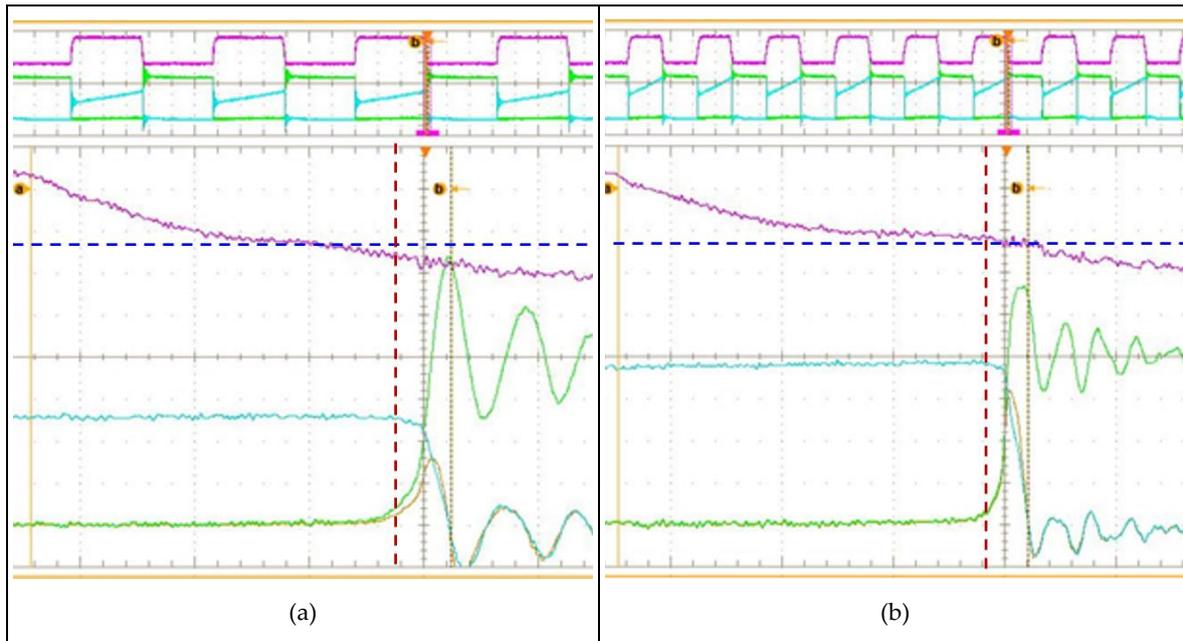
**Figure 5.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off of a 3L MOSFET at high load – (a)  $R_G=3.9\Omega$  (b)  $R_G=15\Omega$ .



**Figure 6.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off of a 4L MOSFET at low load – (a)  $R_G=3.9\Omega$  (b)  $R_G=15\Omega$ .



**Figure 7.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off of a 4L MOSFET at medium load – (a)  $R_G=3.9\Omega$  (b)  $R_G=15\Omega$ .



**Figure 8.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off of a 4L MOSFET at high load – (a)  $R_G=3.9\Omega$  (b)  $R_G=15\Omega$ .

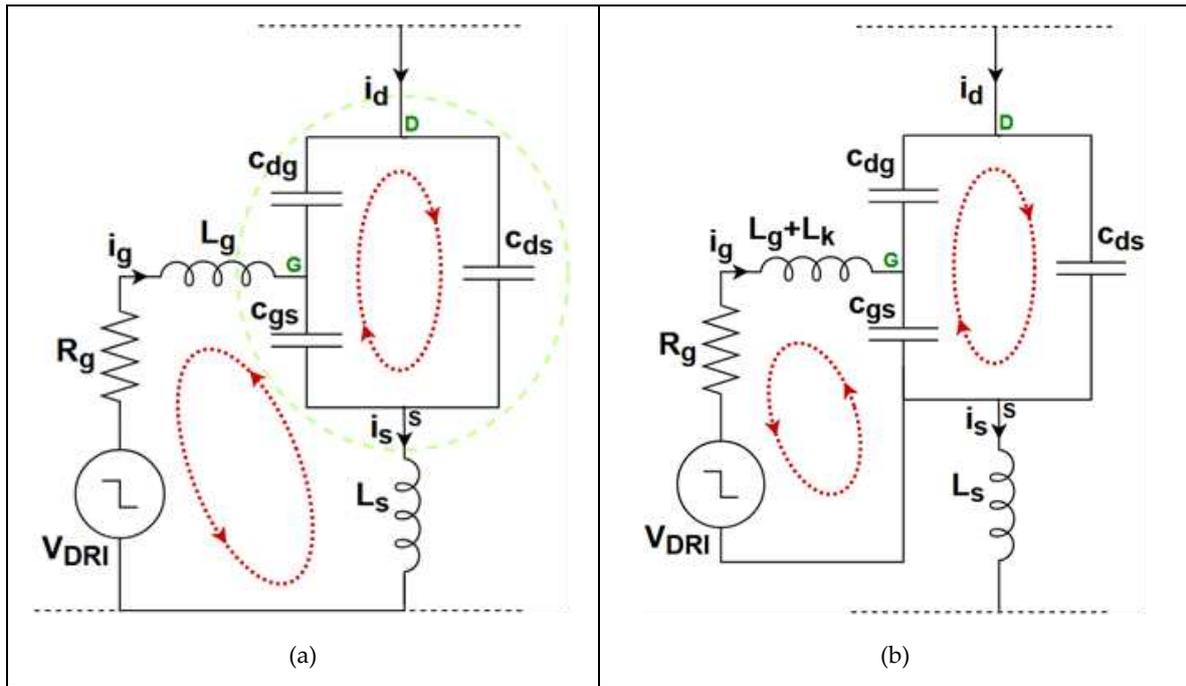
In each figure, a dashed blue line representing the voltage threshold has been added. The value of the voltage threshold accounts for its reduction with increasing MOSFET temperature, being the temperature measured in each specific operating condition reported in the figures. The dashed red line indicates where the switching losses start. Looking at the intersection between the two dashed lines, it arises that the device's gate-source voltage (violet waveform) is below or just above the threshold voltage at the beginning (red dashed line) of the interval where the switching losses are greater than zero. Moreover, when the gate-source voltage is greater than the threshold voltage at the beginning (red dashed line), for a large part of the interval where the power losses are greater than zero the gate-source voltage is lower than the threshold one.

Therefore, the device can be modelled considering only its parasitic capacitance for the circuit analysis.

### 3. Turn-off circuit analysis

As reported in the literature and shown in Figure 2, the additional turn-off switching losses in 3L MOSFET in comparison to the 4L MOSFET increase with increasing gate resistance and load. Such greater switching losses are commonly attributed to the lower switching speed of 3L MOSFET. Therefore, circuit analysis is performed in this section to obtain an analytical formulation of the current slew rate during the turn-off of 3L and 4L MOSFETs. The goal is the identification of an equation representing the effect of the gate resistance and load condition on the current slew rate for comparison purposes.

Figure 9 reports a circuit model of a 3L and 4L MOSFET embedded in the converter. According to the previous considerations based on the analysis of the waveforms, the gate-source voltage has been considered equal or below the threshold and, consequently, the voltage-controlled current generator between the drain and source is absent.



**Figure 9.** Circuit representation of the MOSFET when its current is decreasing (a) 3L (b) 4L.

From the inspection of Figure 9, it is apparent that the following Kirchhoff current laws (KCL) are valid for both MOSFETs.

$$i_d - c_{ds} \frac{dv_{ds}}{dt} - c_{dg} \frac{dv_{dg}}{dt} = 0 \quad (1)$$

$$i_g - c_{gs} \frac{dv_{gs}}{dt} + c_{dg} \frac{dv_{gd}}{dt} = 0 \quad (2)$$

Moreover, looking at the device parasitic capacitances loop, also the following Kirchhoff voltage law (KVL) can be considered for both MOSFETs.

$$v_{dg} + v_{gs} - v_{ds} = 0 \quad (3)$$

By substituting this KVL in equation (1) and rearranging it, the following expression is obtained for both devices:

$$\frac{dv_{gs}}{dt} = \frac{(c_{ds} + c_{dg}) \frac{dv_{ds}}{dt} - i_d}{c_{dg}} \quad (4)$$

Similarly, by substituting the KVL in equation (2) and considering equation (4), the following expression is obtained for the gate current of both MOSFETs:

$$i_g = \frac{c_{gs}(c_{ds} + c_{dg}) + c_{dg}c_{ds}}{c_{dg}} \frac{dv_{ds}}{dt} - \left( \frac{c_{gs} + c_{dg}}{c_{dg}} \right) i_d \quad (5)$$

There is a key difference when the KVL related to the driving loop is considered:  
KVL – 3L (Figure 9a)

$$L_s \frac{di_s}{dt} + v_{gs} + L_g \frac{di_g}{dt} + R_g i_g - V_{DRI} = 0 \quad (6)$$

KVL – 4L (Figure 9b)

$$v_{gs} + (L_g + L_k) \frac{di_g}{dt} + R_g i_g - V_{DRI} = 0 \quad (7)$$

Equations (6) and (7) can be, respectively, combined with the previous one to obtain the analytical expression of the current slew rate. Indeed, in the case of a 3L MOSFET, an additional equation is necessary because the source current is present in equation (6). The necessary additional

equation is obtained considering the KCL related to the Gaussian surface represented by the dashed green line in Figure 9a:

$$i_d + i_g - i_s = 0 \quad (8)$$

By substituting equations (5) and (8) in equation (6) and rearranging the results, the following expression is obtained for the current slew rate of a 3L MOSFET during the turn-off.

$$\frac{di_d}{dt}_{3L} = \frac{c_{dg}(v_{gs}-V_{DRI})+(L_s+L_g)(c_{gs}(c_{ds}+c_{dg})+c_{dg}c_{ds})\frac{d^2v_{ds}}{dt^2}+R_g(c_{gs}(c_{ds}+c_{dg})+c_{dg}c_{ds})\frac{dv_{ds}}{dt}-R_g(c_{gs}+c_{dg})i_d}{L_s c_{gs}+L_g(c_{gs}+c_{dg})} \quad (9)$$

A similar equation can be obtained for the current slew rate of a 4L MOSFET by substituting equation (5) in equation (7) and rearranging the results as reported in equation (10).

$$\frac{di_d}{dt}_{4L} = \frac{c_{dg}(v_{gs}-V_{DRI})+(L_g+L_k)(c_{gs}(c_{ds}+c_{dg})+c_{dg}c_{ds})\frac{d^2v_{ds}}{dt^2}+R_g(c_{gs}(c_{ds}+c_{dg})+c_{dg}c_{ds})\frac{dv_{ds}}{dt}-R_g(c_{gs}+c_{dg})i_d}{(L_g+L_k)(c_{gs}+c_{dg})} \quad (10)$$

In both cases, some considerations enable simplified, although less accurate, equations. In particular:

$$\begin{aligned} \left| (L_s + L_g) \frac{d^2 v_{ds}}{dt^2} \right| &\ll \left| R_g \frac{dv_{ds}}{dt} \right| \\ \left| (L_k + L_g) \frac{d^2 v_{ds}}{dt^2} \right| &\ll \left| R_g \frac{dv_{ds}}{dt} \right| \\ c_{gs} &\gg c_{dg} \\ c_{ds} &\gg c_{dg} \end{aligned}$$

By applying these relations, equations (9) and (10) can be approximated, respectively, as follows:

$$\frac{di_d}{dt}_{3L} \approx \frac{\frac{c_{dg}}{c_{gs}}(v_{gs}-V_{DRI})+R_g c_{ds} \frac{dv_{ds}}{dt}-R_g i_d}{L_s+L_g} \quad (11)$$

$$\frac{di_d}{dt}_{4L} \approx \frac{\frac{c_{dg}}{c_{gs}}(v_{gs}-V_{DRI})+R_g c_{ds} \frac{dv_{ds}}{dt}-R_g i_d}{L_g+L_k} \quad (12)$$

These simplified equations present the same numerator while the denominator is different. The denominators in (11) and (12) represent the total inductance of the driver loop when, respectively, a 3L and a 4L MOSFET are considered. The greatest inductance in the first cases is due to the longer path, then:

$$L_s > L_k \quad (13)$$

$$\frac{1}{L_s+L_g} < \frac{1}{L_g+L_k} \quad (14)$$

Considering equation 14, and considering that the current slew rate is negative during the turn-off, then the term  $-R_g i_d < 0$  in equations (11) and (12) highlights that the current slew rate increases as the gate resistance and current increase. More specifically, the improvement achieved by 4L as the  $R_g$  and  $i_d$  increase can be expressed using the following function:

$$f_{imp}(R_g i_d) = \left| \frac{-R_g i_d}{L_g+L_k} \right| - \left| \frac{-R_g i_d}{L_s+L_g} \right| > 0 \quad (15)$$

which is concordant with the experimental analysis reported in Figure 2. The increment is not linear, and it is negligible at low load due to the term  $R_g c_{ds} \frac{dv_{ds}}{dt}$ , in equations (11) and (12), which is opposite to the current reduction, and it depends on the gate resistance too.

These results are concordant with the experimental switching waveforms reported in Figures 3–8 and highlight the reasons behind the different switching speeds.

To verify experimentally the results obtained in equations (11) and (12), an inductor,  $L_A$ , has been added to the gate path of the 4L MOSFET in Figure 9b, so that:

$$L_{G,new} = L_G + L_A \quad (16)$$

The value of  $L_A$  has been properly chosen to obtain the same driving loop inductance

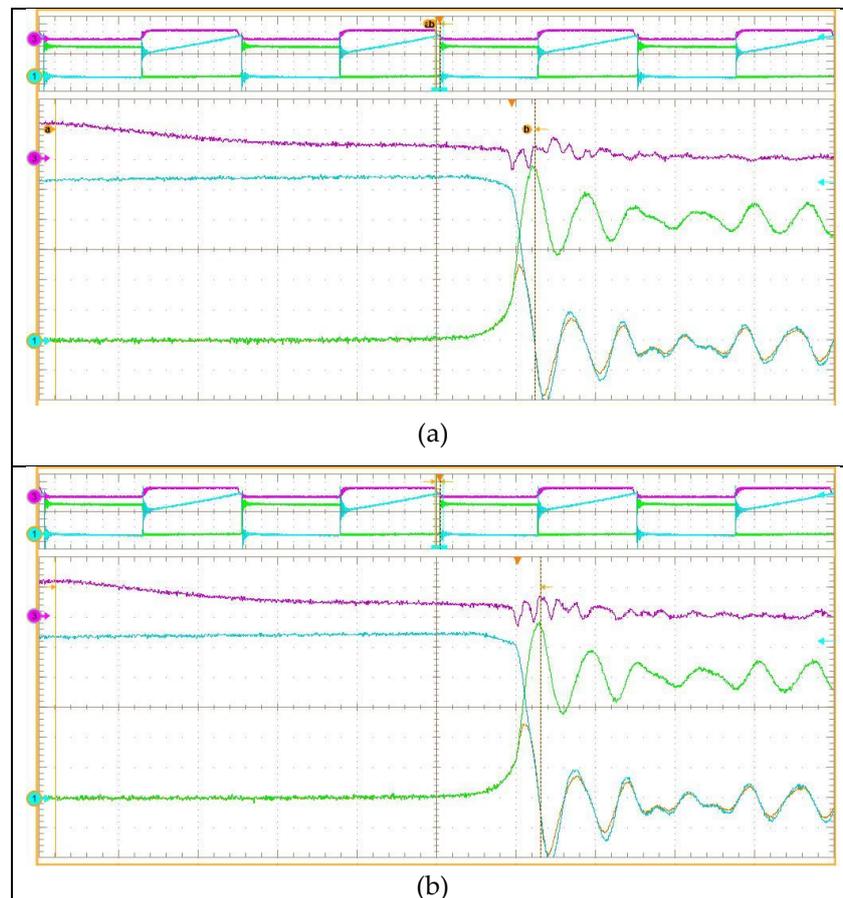
$$L_A = L_S - L_K \quad (17)$$

Under this condition, the current slew rate of the 3L and 4L MOSFETs should be similar if the theoretical aspects obtained in equations (11) and (12) are true:

$$\frac{di_d}{dt}_{4L} \approx \frac{di_d}{dt}_{3L} \quad (18)$$

In other terms, proving equation 18 is sufficient to prove equations (11) and (12).

Figures 10 show the waveforms obtained for 3L (a) and 4L (b) when  $L_A$  is added to the gate path of the 4L MOSFET in Figure 9b, and its inductance has been chosen according to equation 17. The figures confirm that, under this condition the current slew rate is similar, thus proving the theoretical results.



**Figure 10.** Gate-source voltage (purple), drain-source voltage (green) and drain current (light blue) during the turn-off under similar driver loop inductance - (a) 3L (b) 4L.

## 5. Conclusions

The SuperJunction MOSFETs empowered by the addition of the Kelvin pin - 4L MOSFETs - present lower switching losses than the 3L counterpart. The maximum difference between the switching losses of the two MOSFETs is obtained at a high load. This makes the 4L MOSFETs the best choice in high-power density applications when substantial load currents have to be considered.

In this work, the turn-off switching losses of 3L and 4L MOSFETs have been first experimentally compared. Then, circuit models and Kirchhoff laws have been adopted to obtain simplified analytical expressions of the MOSFETs' current slew rate.

These expressions have highlighted the reasons behind the improvements obtained by adopting 4L MOSFET during the turn-off. The key information that emerged is that the turn-off improvement obtained by adopting the Kelvin source is due to the lower inductance of the driver loop in comparison with the power loop inductance instead of the decoupling between these loops. This result has also been experimentally confirmed by adding an inductor to the gate loop of the 4L to achieve a similar total inductance drive loop for 3L e 4L. Under this condition, the same current slew rate has been found, thus confirming the theoretical expressions.

Finally, the circuit analysis and the aforementioned expressions have explained the reasons behind the increment of the difference of the turn-off losses between 3L and 4L with increasing the gate resistance and load current.

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**Conflicts of Interest:** "The authors declare no conflict of interest."

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