A Novel Symmetrical Active-Switched Coupled-Inductor High-Step-Up DC/DC Converter

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Article

A Novel Symmetrical Active-Switched Coupled-Inductor High-Step-Up DC/DC Converter

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Abstract: This paper proposes a novel symmetrical active-switched coupled-inductor high-step-up DC/DC converter. A new active-switched coupled inductor is used to allow much higher voltage gain of the proposed converter. The symmetrical circuit structure of the proposed converter evenly divides large input currents and reduce input current ripple by operating in interleaved mode so power density is increased. The switches also have low voltage stress. The operating principle and design considerations for the converter topology are described. The proposed converter with an input voltage of 40 V, an output voltage of 400 V and an output of 1000 W at a switching frequency of 50 kHz is implemented. The simulations and experimental results are thus depicted to verify the theoretical analysis. The highest efficiency is 95.5% at 200 W measured by using a HIOKI 3390. Consequently, the proposed converter is suitable for renewable energy generation systems that require high power, high voltage gain and high efficiency.

Keywords: High Step-Up DC-DC Converter; Active-Switched Coupled Inductor; Interleaved Operation

1. Introduction

Due to the energy crisis caused by the problem of global warming, energy saving and carbon reduction become much more important. Renewable energy applications, including solar, wind or fuel cells, are thus emphasized because they have zero carbon emissions. For a single-phase 220 Vac generated from a DC-AC inverter in a distributed power grid system with renewable energy, a high dc voltage of 380~420 V is required to offer to the inverter. However, the output voltage of a solar array module is about 36 ~ 48 V for domestic applications, so a step-up DC-DC converter with a high voltage gain is needed to convert the voltage level.

In general, the ideal traditional boost DC-DC converter with a near unity duty cycle can achieve high voltage gain, but the presence of parasitic resistances in circuit components greatly limits the voltage gain and conversion efficiency [1]. Therefore, for obtaining a high voltage gain and improving the conversion efficiency, many high step-up techniques have been presented and applied to propose a lot of high step-up converter structures [2–26].

Switched-capacitor techniques [2–7] and voltage-lift techniques [8–16] have been widely used to achieve high step-up voltage gain. The main purpose for these step-up techniques is to create voltages across the capacitors. Therefore, the induced capacitor voltages can be positively series at output side for a very high output voltage, but some of the high step-up converters [3,8,17] have the drawback of no common ground involving the load, switches, and the input voltage source in order to cascode the voltages from the equivalent circuit structure deformed by component displacement. On the other hand, the capacitor voltages can also be set as a negative voltage against output voltage in the path of releasing energy for the inductor when the switch is off to be able to derive a much higher output voltage based on volt–second balance principle to inductors. However, if the voltage gain needs to be increased in advance, much more diodes and capacitors will be required and result in more cost and power losses. On the other hand, the high charging currents will also exist and flow through the main switches and rectified diodes, and that will increase more power dissipation.

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In order to increase the voltage conversion ratio of a dc–dc converter, the other common solution is to use the turns ratio of the coupled inductor or transformer [17–19]. These high step-up converters have an extra design freedom degree, which is the turns ratio. High voltage gain can thus be achieved for these converters with high turns ratio. However, a large turns ratio increases leakage inductance, which may cause high voltage spikes and increases voltage stresses on the switches and diodes. Therefore, several non-isolated converters have been proposed, such as switched-inductor applications [20–26].

In [26], a symmetrical dual-switch converter with synchronous switching mode is presented. It has a simple circuit configuration and can achieve a high voltage gain based on the switched-inductor boost technique. But a high voltage stresses of switches, high input current ripple and just one degree of design freedom are the main drawbacks. However, in this paper, an active-switched coupled-inductor can be proposed and applied in this symmetrical dual-switch circuit structure, and thus a voltage multiplier [17,18,20,23] can also be used to achieve much higher voltage gain and decrease the voltage stresses of the switches and diodes in the proposed active-switched coupled-inductor high-step-up DC/DC converter as shown in Figure 1. On the other hand, the proposed converter operated in interleaved mode can also obtain the lower input current ripple. The advantages of the proposed converters are thus demonstrated as follows.

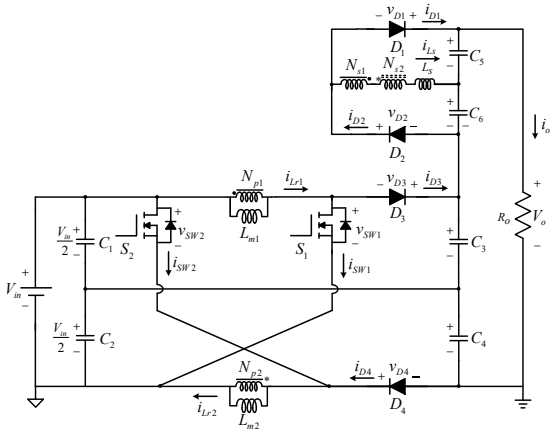

Figure 1. Proposed converter

(1) **Simple and innovative topology:** The symmetrical circuit structure is simple and the components are few. The new active-switched coupled-inductor boost technology features both switching inductor and coupled inductor boost characteristics so the converter can be easier to achieve a higher voltage gain.

(2) **High voltage gain:** The converter has a high boost voltage conversion ratio without an extremely large duty cycle and the turns ratio n is used to allows a high voltage gain and much freedom of design.

(3) **High-power applications:** For renewable energy power generation systems, the input voltage is usually low so there is a large input current for the high-power applications. The symmetric structure of the proposed converter using an interleaved operation can share the large input current and reduce input current ripple, simultaneously. This paper proposes a converter with an output power of 1 kW.

(4) **Low voltage stress:** For a specific power application, due to the symmetrical circuit structure and the active-switched coupled-inductor high-step-up technique for the proposed converter, the voltage stress on the switches is much less than the output voltage of 400 V.

(5) **High efficiency:** The interleaved operation and symmetrical structure reduces the voltage and current stress on the switches and diodes, so switches with low ON-resistance and diodes with low forward voltage are used to reduce conduction losses and increase overall efficiency. The maximum efficiency for the converter is 95.5%.

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2. Proposed Converter and Operating Principle

The proposed converter is shown in Figure 1. S_1 and S_2 are power switches, L_{m1} and L_{m2} are magnetizing inductors and N_{p1} , N_{p2} , N_{s1} and N_{s2} are the number of turns in the primary and secondary coils, respectively. D_1 and D_2 are voltage-doubling diodes, D_4 and D_5 are clamping diodes, C_1 and C_2 are input capacitors, C_3 and C_4 are clamping capacitors, C_5 and C_6 are voltage-doubling capacitors, V_{in} is the input voltage, V_o is the output voltage and R_o is the output load.

The theoretical key waveforms for proposed converter operating in continuous conduction mode (CCM) are shown in Figure 2. The proposed converter has six linear stages during one switching cycle. The equivalent circuits for these stages are shown in Figure 3.

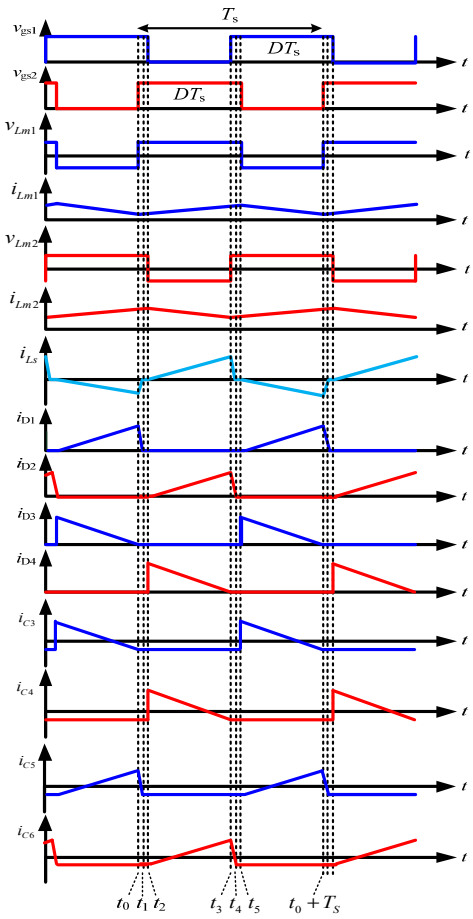

Figure 2. Theoretical key waveform for the proposed converter operating in CCM

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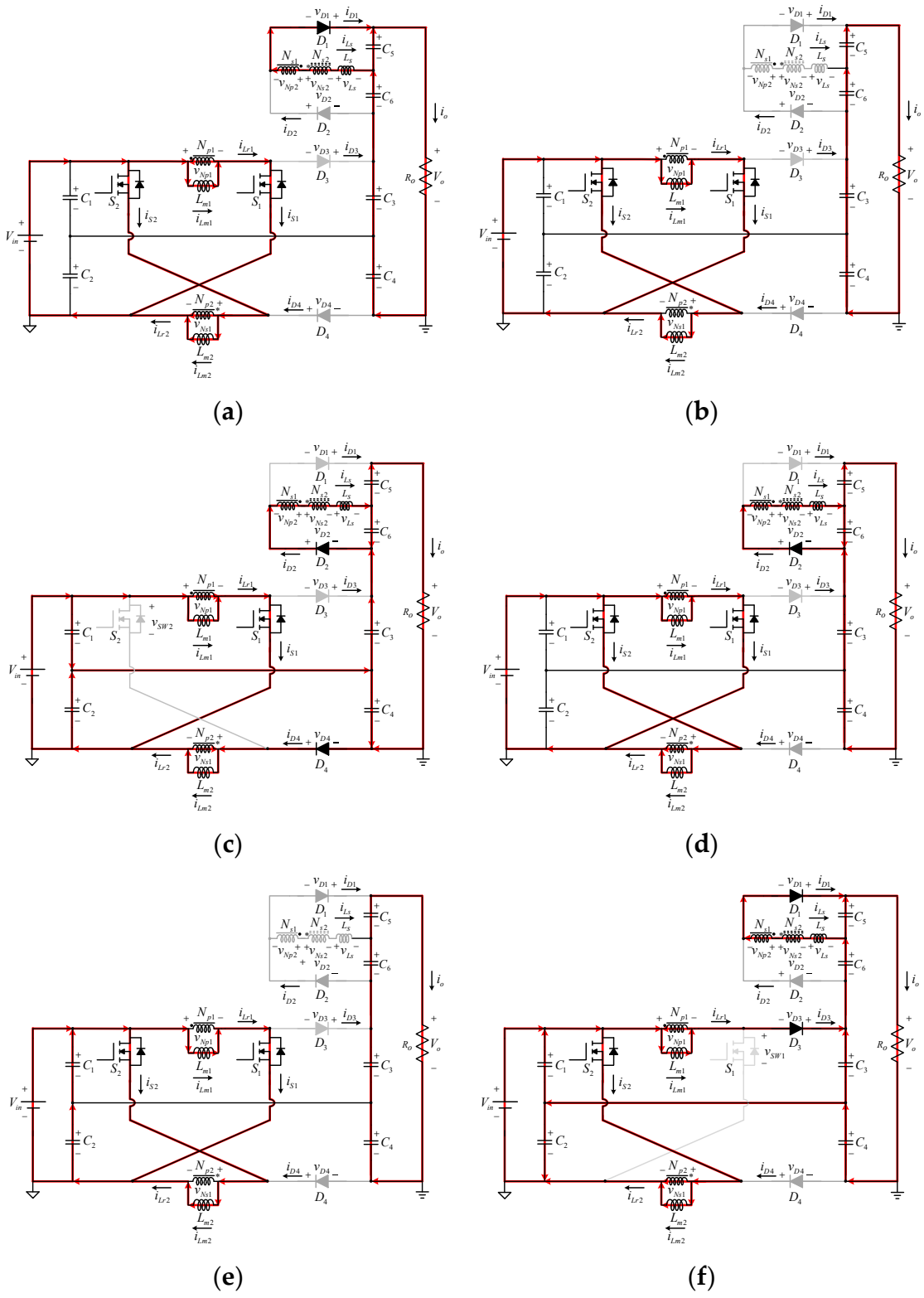

Figure 3. Equivalent circuits for: (**a**) Stage 1, (**b**) Stage 2, (**c**) Stage 3, (**d**) Stage 4, (**e**) Stage 5 and (**f**) Stage 6.

The following assumptions are made before the theoretic analyzing.

(1) The converter is operating in a steady-state.

(2) The magnetizing inductors L_{m1} and L_{m2} are assumed to be sufficiently large to allow the magnetizing inductor current to operate in continuous conduction mode (CCM).

(3) Inductors, capacitors, power switches and diodes are ideal.

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(4) C_1, C_2, C_3, C_4, C_5, and C_6 are sufficiently large that the voltage is regarded as constant within one switching cycle.

Stage 1 **[**$t_0 \sim t_1$**]:** This stage starts at $t = t_0$, when power switches S_1 and S_2 are turned on. Diodes D_2, D_3 and D_4 are turned off due to the reverse-bias. Diode D_1 remains on due to discharge of the leakage inductor current i_{Ls}. The path for current flow is shown in Figure 3a. The voltages across the inductors at this stage are:

$$\begin{cases} v_{Lm1} = V_{in} \\ v_{Lm2} = V_{in} \end{cases} \tag{1}$$

$$v_{Ls} = v_{Np2} - v_{Ns2} + V_{C5} = nv_{Np1} - nv_{Ns1} + V_{C5} = V_{C5} \tag{2}$$

Inductor currents i_{Lm1}, i_{Lm2} and i_{Ls} all increase linearly and the reverse-bias for diodes D_2, D_3 and D_4 is:

$$\begin{cases} v_{D2} = V_{C5} + V_{C6} \\ v_{D3} = V_{C3} + V_{C2} \\ v_{D4} = V_{C4} + V_{C1} \end{cases} \tag{3}$$

As the leakage inductor current i_{Ls} increases to zero at $t = t_1$, D_1 is turned off and the next stage begins.

Stage 2 **[**$t_1 \sim t_2$**]:** This stage starts at $t = t_1$. Power switches S_1 and S_2 are still on. Diodes D_1, D_2, D_3 and D_4 become reverse-bias. The path for current flow is shown in Figure 3b. The voltages across inductors at this stage are:

$$\begin{cases} v_{Lm1} = V_{in} \\ v_{Lm2} = V_{in} \end{cases} \tag{4}$$

$$v_{Ls} = 0 \tag{5}$$

Inductor currents i_{Lm1} and i_{Lm2} both increase linearly and i_{Ls} remains at zero. The voltages across diodes D_1, D_2, D_3, and D_4 are:

$$\begin{cases} v_{D1} = V_{C5} \\ v_{D2} = V_{C6} \\ v_{D3} = V_{C3} + V_{C2} \\ v_{D4} = V_{C4} + V_{C1} \end{cases} \tag{6}$$

If $t = t_2$, power switch S_2 is turned from on to off and this stage ends.

Stage 3 **[**$t_2 \sim t_3$**]:** This stage starts at $t = t_2$. Power switch S_2 is turned off, and the power switch S_1 still on. Diodes D_1 and D_3 are still off due to the reverse-bias. The magnetizing inductor current i_{Lm2} decreases and inductor L_{m2} is discharged to the load through D_2 and D_4 so the diodes D_2 and D_4 are forced to conduct. The path for current flow is shown in Figure 3c. The voltages across the inductors at this stage are:

$$\begin{cases} v_{Lm1} = V_{in} \\ v_{Lm2} = \dfrac{V_{in}}{2} - V_{C4} < 0 \end{cases} \tag{7}$$

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$$v_{Ls} = v_{Np2} - v_{Ns2} - V_{C6} = nv_{Np1} - nv_{Ns1} - V_{C6} = nV_{in} - n\left(\frac{V_{in}}{2} - V_{C4}\right) - V_{C6} > 0 \tag{8}$$

Inductor currents i_{Lm1} and i_{Ls} still increase linearly and i_{Lm2} decreases linearly. At this stage, the voltage across power switch S_2 is:

$$v_{S2} = V_{C1} + V_{C4} \tag{9}$$

The reverse-bias voltages for diodes D_1 and D_3 are:

$$\begin{cases} v_{D1} = V_{C5} + V_{C6} \\ v_{D3} = V_{C2} + V_{C3} \end{cases} \tag{10}$$

At $t = t_3$, power switch S_2 is turned on again and this stage ends and the next stage begins.

Stage 4 **[** $t_3 \sim t_4$ **]:** This stage starts at $t = t_3$, when power switch S_2 is turned on and power switch S_1 remains on. At this time, diode D_4 is turned off due to the reverse-bias. The path for current flow is shown in Figure 3d. The voltages across the inductors at this stage are:

$$\begin{cases} v_{Lm1} = V_{in} \\ v_{Lm2} = V_{in} \end{cases} \tag{11}$$

$$v_{Ls} = v_{Np2} - v_{Ns2} - V_{C6} = nv_{Np1} - nv_{Ns1} - V_{C6} = -V_{C6} < 0 \tag{12}$$

Inductor currents i_{Lm1} and i_{Lm2} increase linearly and i_{Ls} decreases linearly. At this time, the reverse-bias voltages across diodes D_1, D_3 and D_4 are:

$$\begin{cases} v_{D1} = V_{C5} + V_{C6} \\ v_{D3} = V_{C3} + V_{C2} \\ v_{D4} = V_{C4} + V_{C1} \end{cases} \tag{13}$$

At $t = t_4$, the leakage inductor current i_{Ls} is reduced to zero so D_2 is turned off and the next stage begins.

Stage 5 **[** $t_4 \sim t_5$ **]:** This stage starts at $t = t_4$. Power switches S_1 and S_2 remain on, and diodes D_2, D_3 and D_4 are off. The path for current flow is shown in Figure 3e. The operation for this stage is exactly the same as that for Stage 2, so it is not described in detail again at this stage. At $t = t_5$, power switch S_1 is turned off and this stage ends and the next begins.

Stage 6 **[** $t_5 \sim t_0 + T_S$ **]:** This stage starts at $t = t_5$. Power switch S_1 is turned off, power switch S_2 remains on, and diodes D_2 and D_4 are both off. The magnetizing inductor current i_{Lm1} begins to decrease and inductor L_{m1} is discharged to the load through D_1 and D_3 so diodes D_1 and D_3 are forced to conduct. The path for current flow is shown in Figure 3f. The voltage across the inductors at this stage is:

$$\begin{cases} v_{Lm1} = \dfrac{V_{in}}{2} - V_{C3} < 0 \\ v_{Lm2} = V_{in} \end{cases} \tag{14}$$

$$v_{Ls} = -v_{Np2} + v_{Ns2} + V_{C5} = -nv_{Np1} + nv_{Ns1} + V_{C5} = -n\left(\frac{V_{in}}{2} - V_{C3}\right) nV_{in} + V_{C5} < 0 \tag{15}$$

Inductor currents i_{Lm1} and i_{Ls} decrease linearly and i_{Lm2} increases linearly. At this stage, the voltage across power switch S_1 is:

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$$v_{S1} = V_{C2} + V_{C3} \tag{16}$$

The voltage across diodes D_2 and D_4 is:

$$\begin{cases} v_{D2} = V_{C5} + V_{C6} \\ v_{D4} = V_{C1} + V_{C4} \end{cases} \tag{17}$$

When $t = t_0 + T_S$, power switch S_1 is turned on again to complete one switching cycle for the circuit.

3. Steady-State Analysis

This section analyzes the converter's voltage gain ratio, component voltage stress and the design conditions for inductors and capacitors in a steady state. At last, the performance comparison with some high step-up converters in literature is also presented herein.

3.1. Voltage Gain Ratio Derivation

Applying the volt–second balance principle to magnetizing inductors L_{m1} and L_{m2}, the voltage across capacitors C_3 and C_4 is:

$$\begin{cases} \langle v_{Lm1} \rangle_{T_s} = 0 \\ \langle v_{Lm2} \rangle_{T_s} = 0 \end{cases} \Rightarrow \begin{cases} DV_{in} + (1-D)\left(\frac{V_{in}}{2} - V_{C3}\right) = 0 \\ DV_{in} + (1-D)\left(\frac{V_{in}}{2} - V_{C4}\right) = 0 \end{cases} \Rightarrow V_{C3} = V_{C4} = \frac{1+D}{1-D}\frac{V_{in}}{2} \tag{18}$$

To simplify the analysis, the leakage inductor is ignored for Stages 3 and 6, so the voltage across capacitors C_5 and C_6 is:

$$\begin{cases} V_{C6} = v_{Np2} - v_{Ns2} = nV_{in} - n\left(\frac{V_{in}}{2} - V_{C4}\right) \\ V_{C5} = v_{Np2} - v_{Ns2} = nV_{in} - n\left(\frac{V_{in}}{2} - V_{C3}\right) \end{cases} \tag{19}$$

Substituting (18) into (19) gives:

$$V_{C5} = V_{C6} = \frac{n}{(1-D)}V_{in} \tag{20}$$

By using Equations (18) and (20), the voltage gain ratio for the converter is calculated as:

$$M = \frac{V_o}{V_{in}} = \frac{V_{C3} + V_{C4} + V_{C5} + V_{C6}}{V_{in}} = \frac{(1+D)+2n}{1-D} \tag{21}$$

There are two design conditions that affect the voltage gain for the converter: the coupled turns ratio n and the duty cycle D. There are two degrees of freedom in the voltage-gain design. Appropriate values for n and D ensure that there is a high voltage gain without using a extremely duty cycle.

The voltage gain curve for the proposed converter is shown in Figure 4. If either the duty cycle or the turns ratio is increased, the voltage gain increases. If the turns ratio of the coupled inductor is $n=1$, the voltage gain is 10 with $D=0.636$ and if the turns ratio for the coupled inductor is $n=3$, the voltage gain can achieve 20 with $D=0.619$.

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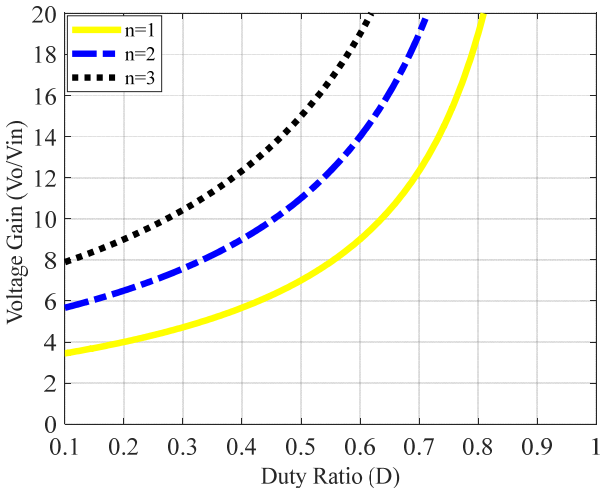

Figure 4. Voltage gain for the proposed converter versus turns ratio n and duty cycle D .

3.2. Voltage Stresses on Semiconductor Devices

When power switches S_1 and S_2 are off, the voltage stresses are calculated as:

$$v_{S1(votage-stress)} = V_{C2} + V_{C3} = \frac{1}{(1-D)} V_{in} = \frac{1}{(1+D)+2n} V_o \tag{22}$$

$$v_{S2(votage-stress)} = V_{C1} + V_{C4} = \frac{1}{(1-D)} V_{in} = \frac{1}{(1+D)+2n} V_o \tag{23}$$

When the diodes are off, the voltage stresses are:

$$v_{D1(votage-stress)} = V_{C5} + V_{C6} = \frac{2n}{(1-D)} V_{in} = \frac{2n}{(1+D)+2n} V_o \tag{24}$$

$$v_{D2(votage-stress)} = V_{C5} + V_{C6} = \frac{2n}{(1-D)} V_{in} = \frac{2n}{(1+D)+2n} V_o \tag{25}$$

$$v_{D3(votage-stress)} = V_{C2} + V_{C3} = \frac{1}{(1-D)} V_{in} = \frac{1}{(1+D)+2n} V_o \tag{26}$$

$$v_{D4(votage-stress)} = V_{C1} + V_{C4} = \frac{1}{(1-D)} V_{in} = \frac{1}{(1+D)+2n} V_o \tag{27}$$

3.3. Design of Inductors

Assuming the current sharing is achieved, the currents of magnetizing inductors L_{m1} and L_{m2} are the same after one of those currents are shifted half switching period. I_{Lm} is the average current of magnetizing inductors L_{m1} and L_{m2} , and Δi_{Lm} is the inductor ripple current. When the converter operates in CCM. It shows that

$$I_{Lm} > \frac{1}{2} \Delta i_{Lm} \tag{28}$$

The average magnetizing inductor current is half of the average input current. It yields

$$I_{Lm} = I_{Lm1} = I_{Lm2} = \frac{P_o}{2V_{in}} \tag{29}$$

where P_o is the average output power. The inductor current ripple Δi_{Lm} is written as:

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$$\Delta i_{Lm} = \frac{V_{in} D T_s}{L_m} \tag{30}$$

Substituting (29)-(30) into (28) gives the design condition for inductor L_m as:

$$L_m > \frac{V_{in}^{\,2} \cdot R_o \cdot D T_s}{V_o^{\,2}} \tag{31}$$

3.4. Design of Capacitors

Based on the charges for capacitors through the circuit in Figure 2, it gives:

$$\begin{cases} C_3 \Delta V_{C3} = \dfrac{V_o (1-D) T_s}{R_o} \\ C_4 \Delta V_{C3} = \dfrac{V_o D T_s}{R_o} \\ C_5 \Delta V_{C3} = \dfrac{V_o (1-D) T_s}{R_o} \\ C_6 \Delta V_{C3} = \dfrac{V_o D T_s}{R_o} \end{cases} \tag{32}$$

The capacitances are calculated using Equation (32) as:

$$\begin{cases} C_3 = \dfrac{V_o (1-D) T_s}{R_o \Delta V_{C3}} \\ C_4 = \dfrac{V_o D T_s}{R_o \Delta V_{C4}} \\ C_5 = \dfrac{V_o (1-D) T_s}{R_o \Delta V_{C5}} \\ C_6 = \dfrac{V_o D T_s}{R_o \Delta V_{C6}} \end{cases} \tag{33}$$

Equations (18), (20) and (21) are substituted into this equation (33) to get:

$$\begin{cases} C_3 = \dfrac{2(1+D+2n)(1-D) T_s}{(1+D) \cdot R_o \cdot (\Delta V_{C3} / V_{C3})} \\ C_4 = \dfrac{2(1+D+2n) D T_s}{(1+D) \cdot R_o \cdot (\Delta V_{C4} / V_{C4})} \\ C_5 = \dfrac{(1+D+2n)(1-D) T_s}{n R_o \cdot (\Delta V_{C5} / V_{C5})} \\ C_6 = \dfrac{(1+D+2n) D T_s}{n R_o \cdot (\Delta V_{C6} / V_{C6})} \end{cases} \tag{34}$$

3.5. Performance Comparison

In this paper, a comparison with three high step-up converters [19–21] is given. The comparison shown in Table 1 includes voltage gain, the value of voltage gain at n=1 and D=0.6, voltage stresses of switches and diodes, number of switches, diodes, capacitors, cores and winding, input current sharing ability, and efficiency at 200-250 W. It shows that the proposed converter has the higher voltage gain of 9 than 7 of converter in [20] and 6.25 of converter in [21]. In order to obtain the same voltage gain, the converters in [20] and [21] are required larger turn ratios or duty cycles, which thereby increase power losses. It also can see that the efficiency 95.5 % of the proposed converter at

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200 W is higher than those 94.3 % and 92 % of the converters in [20] and [21], respectively. In addition, the proposed converter and the converter in [20] have the current sharing ability, but the converter in [21] does not have. It reveals that the current flowing through the components of the converter in [21] is larger than those of the proposed converter and converter in [20], so the converter in [21] has higher conduction losses and worse power efficiency.

On the other hand, by comparing with the proposed converter and the converter in [19], it gives that they can offer the same high voltage gain but the proposed converter has fewer components, resulting in a smaller volume, higher power density, and fewer magnetic cores, reducing volume and magnetic core losses. Moreover, the proposed converter exhibits lower power switch and diode voltage stresses compared to converters [19–21]. Therefore, low conduction resistance switches can be used to reduce conduction losses and costs. This is the reason why the efficiency of the proposed converter is also higher than that of the converter in [19].

Table 1. Comparison of the proposed converter with other previously presented converters.

Parameter	[19]	[20]	[21]	Proposed converter
Voltage gain(M)	$\frac{1+D+2n}{1-D}$	$\frac{1}{1-D}+2n$	$\frac{1}{(1-D)^2}$	$\frac{1+D+2n}{1-D}$
M for n=1, D=0.6	9	7	6.25	9
Voltage stress of switch (V_S/V_{in})	$\frac{M}{1+D+2n}$	$\frac{M}{1+2n-2nD}$	M	$\frac{M}{1+D+2n}$
Maximum voltage stress of diodes (V_D/V_{in})	$\frac{(n+1)M}{1+D+2n}$	$\frac{nM}{1+2n-2nD}$	M	$\frac{2nM}{1+D+2n}$
Number of elements Switches/diodes/ capacitors/cores/ winding	2/4/6/4/4	2/4/3/2/4	2/2/2/2/2	2/4/6/2/4
Input current sharing	Yes	Yes	No	Yes
Efficiency	93.2% @200 W	94.3% @200 W	92% @250 W	95.5% @200 W

4. Controller Design

A controller is designed to regulate the output voltage of the proposed converter with variations in input voltage and load. The control block diagram is shown in Figure 5. T The transfer function $G(s)$ is obtained from the control signal $\tilde{v}_c$ to the output voltage divider signal $K_{fb}\tilde{v}_o$. It is written as:

$$G(s) = K_{fb}P(s)K_{pwm} \tag{35}$$

where the equivalent gain for the PWM (pulse width modulation) circuit is K_{pwm}, the transfer function of proposed converter is $P(s)$, K_{fb} is the feedback voltage gain. Moreover, $C(s)$ is a controller that needs to be designed.

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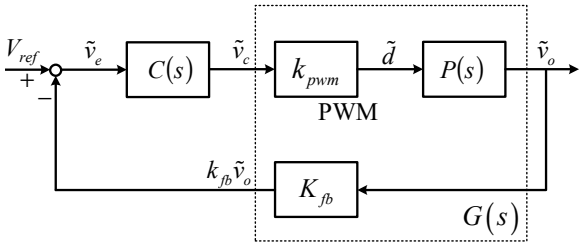

Figure 5. Control block diagram for the overall system.

A prototype converter was constructed and tested. The specifications of the proposed converter and component parameters derived from the design considerations are shown in Table 2. A frequency response analyzer (FRA51602) was used to measure the Bode plots of the plant $G(s)$ for an output power of 500 W. The result is shown in Figure 6. The red curves are the measured results and the blue curves are derived by curve fitting using MATLAB software. It shows that the two curves are similar in terms of gain and phase. Therefore, the small-signal transfer function for the proposed converter is obtained as:

Table 2. Specifications and parameters for the proposed converter.

Parameter/Description	Specification/Value
Input voltage V_{in}	40 V
Output voltage V_o	400 V
Rated output power P_o	1000 W
Switching frequency f_s	50 kHz
Magnetizing inductance L_m	140 μH
Turns ratio n	1
Power switches S_1 and S_2	NTHL020N090SC1
Diodes D_1, D_2, D_3, D_4	STTH3003CW
Capacitor C_1, C_2, C_3, C_4, C_5, C_6	100 μF

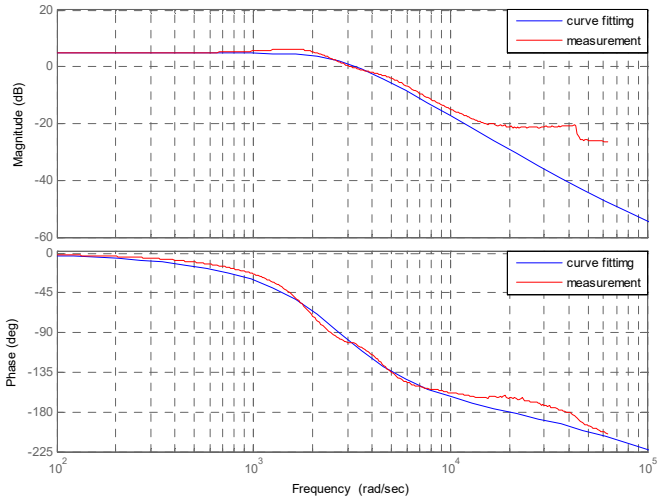

Figure 6. Bode plots for the measurement result (red) and curve fitting result (blue).

$$G(s)=1.74\frac{\left(1-\frac{s}{100000}\right)}{\left(\frac{1}{2800^2}s^2+\frac{2\times0.7}{2800}s+1\right)} \tag{36}$$

Based on (36), the voltage feedback controller is designed by the K-factor method [27]. A 45° phase margin at a crossover frequency of 1 kHz is given that a Type III controller is designed as

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$$C(s)=174825\times\frac{(s+2083)(s+2222)}{s(s+19230)(s+20202)} \tag{37}$$

The Type III controller is implemented using an operational amplifier circuit shown in Figure 7, and the transfer function of the proposed Type-III controller is presented as

$$\frac{\tilde{v}_c(s)}{K\tilde{v}_o(s)}=-\frac{R_1+R_3}{R_1R_3C_2}\frac{\left(s+\frac{1}{R_2C_1}\right)\left(s+\frac{1}{(R_1+R_3)C_3}\right)}{s\left(s+\frac{1}{R_2C_1C_2/(C_1+C_2)}\right)\left(s+\frac{1}{R_3C_3}\right)} \tag{38}$$

From (37) and (38), the passive components of the Type III controller in Figure 7 can be calculated and used to realize the designed controller, where it yields

$$\begin{gathered}R_1=100\ \text{k}\Omega\ 、\ R_2=100\ \text{k}\Omega\ 、\ R_3=11\ \text{k}\Omega\ 、\\ C_1=4.8\ \text{nF}\ 、\ C_2=0.52\ \text{nF}\ 、\ C_1=4.5\ \text{nF}\end{gathered} \tag{39}$$

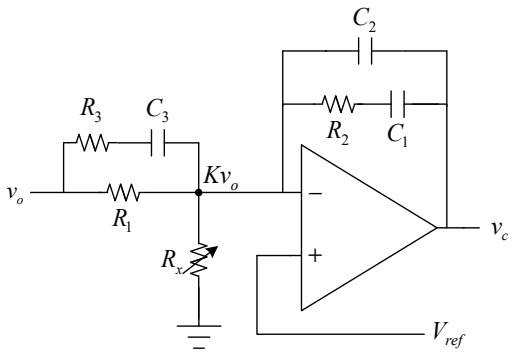

Figure 7. Type III Controller circuit.

Finally, the Bode plots for plant $G(s)$, the Bode plots for the controller $C(s)$ and the Bode plots for the open-loop system $Tol(s)=G(s)C(s)$ can be drawn and shown in Figure 8. It reveals that a 45° phase margin at a crossover frequency of 1 kHz is achieved.

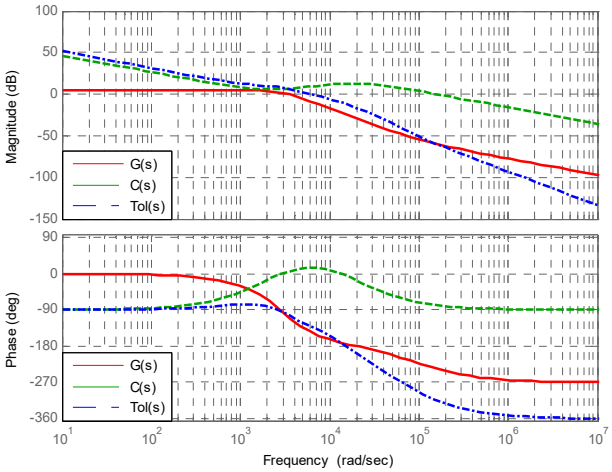

Figure 8. Bode plots for the plant, controller and open-loop system.

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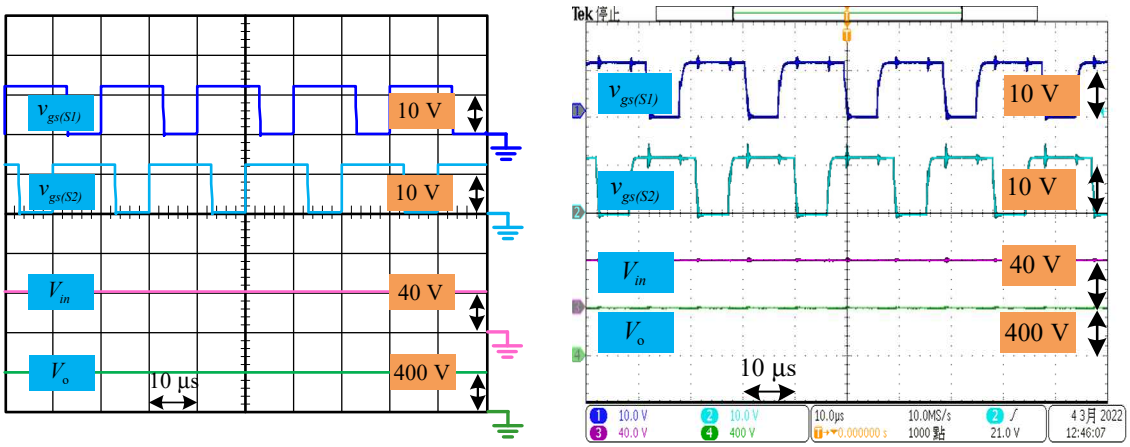
5. Simulations and Experimental Results

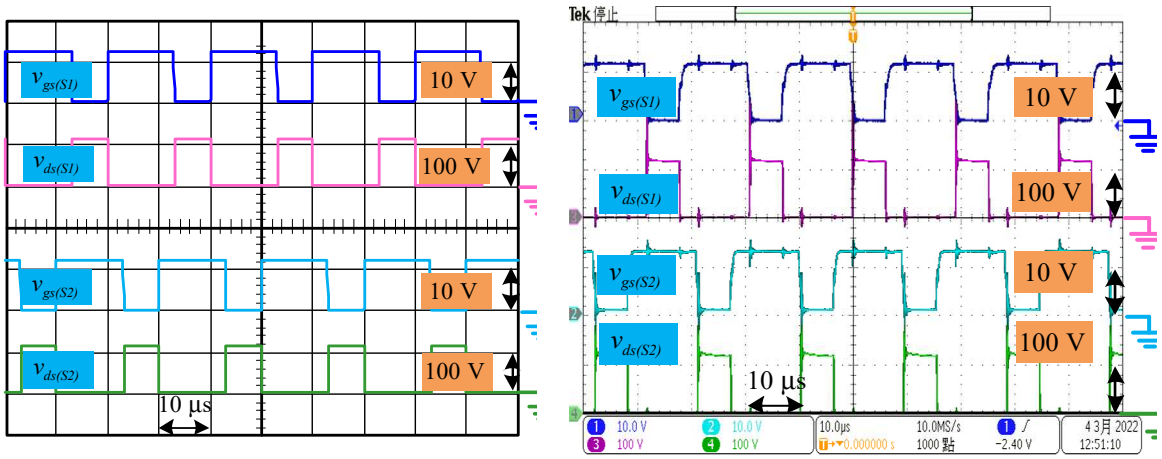
This paper simulates and implements a proposed converter operating at 200-1000 W. Figures 9–13 show the waveforms for the Is-Spice simulations and experimental results for the proposed converter at 1 kW in the steady state.



(a) (b)

Figure 9. Waveforms for v_{gs1}, v_{gs2}, V_{in} and V_o: (**a**) Simulation results. (**b**) Experimental results.

Figure 9 shows that the input voltage V_{in} is 40 V and the output voltage V_o is 400 V. The high voltage gain of 10 is achieved herein. From the drive signals for the switches, it shows that the duty cycle for simulation is 0.643, for experimental result is 0.67. The duty cycle for theoretical value is 0.636 calculated form (21). There is a significant reduction in voltage drop in practice because the actual components are not ideal, so the duty cycle for experimental result is slightly higher than those for simulation and the theoretical result.



(a) (b)

Figure 10. Waveforms for v_{gs1}, v_{gs2}, v_{ds1} and v_{ds2}: (**a**) Simulation results. (**b**) Experimental results.

The waveforms for voltages v_{ds1} and v_{ds2} across power switches S_1 and S_2 are shown in Figure 10. The simulations and experimental results of voltage stresses v_{ds1} and v_{ds2} in steady state are 114 V and 112 V, respectively. Both of them are close to the theoretical results of 110 V. Therefore, the switches for the proposed converter have low voltage stress.

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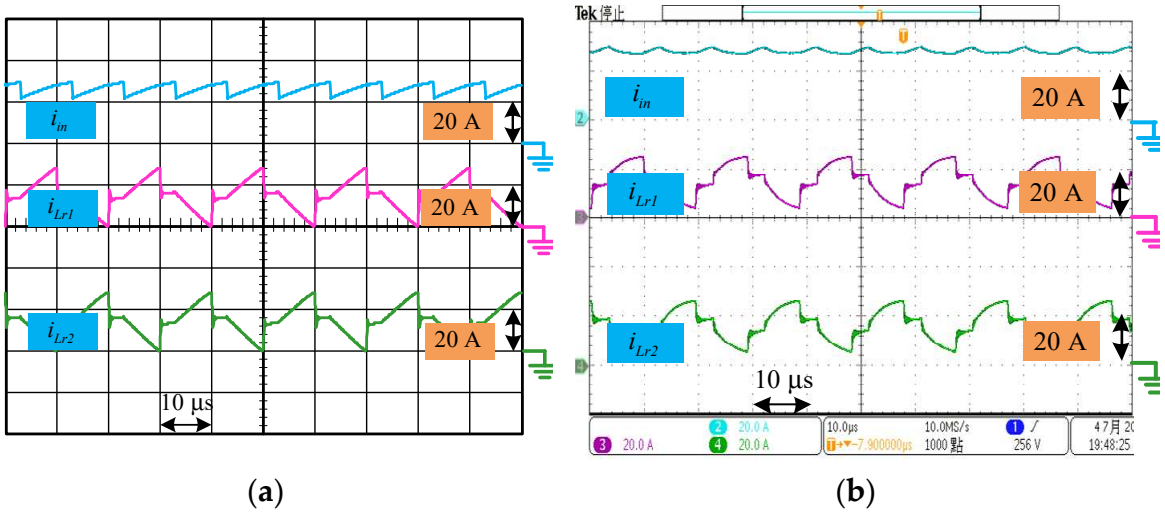

Figure 11. Waveforms for i_{in}, i_{Lr1} and i_{Lr2}: (**a**) Simulation results. (**b**) Experimental results.

The converter is a symmetrical structure and current i_{Lr1} is similar to i_{Lr2} but interleaved with a $180°$ phase shift. The waveforms for input current i_{in}, currents i_{Lr1} and i_{Lr2} are shown in Figure 11. The average currents of i_{Lr1} and i_{Lr2} are the same of 14.2 A for the simulation results and are 14.42 A and 14.52 A respectively for the experiment results. Therefore, the converter features the performance of current sharing. Moreover, it reveals from Figure 11 that the current ripples of the input current i_{in} are 7.74 A and 3.95 A for simulation and experimental result respectively. They become much smaller than the current ripples of i_{Lr1} and i_{Lr2}, which are 27.8 A and 21.4 A for simulation and experimental result respectively.

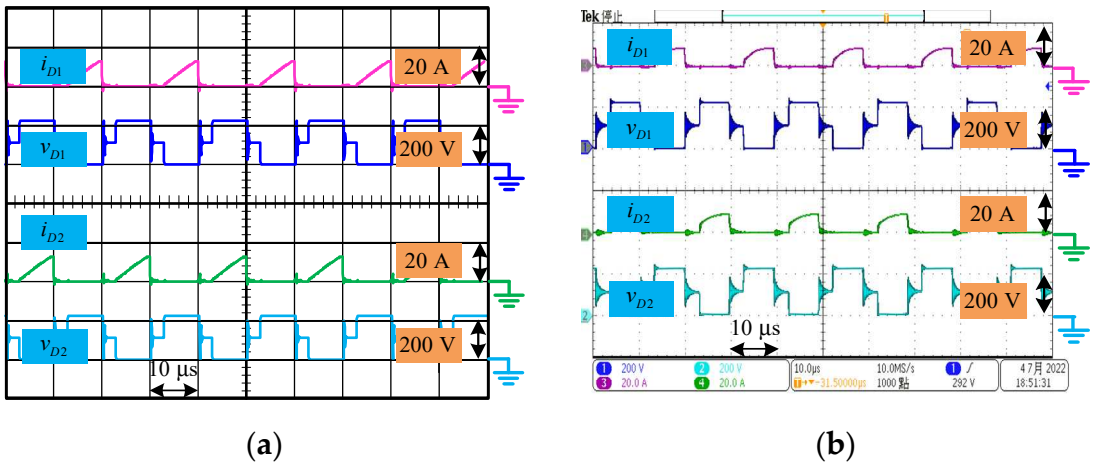

Figure 12. Waveforms for i_{D1}, v_{D1}, i_{D2} and v_{D2}: (**a**) Simulation results. (**b**) Experimental results.

The current and voltage waveforms for diodes D_1 and D_2 are shown in Figure 12. The current and voltage waveforms for diodes D_3 and D_4 are shown in Figure 13. It shows that there is no reverse-recovery problem for all the diodes as diode is turned from on to off. Moreover, it also gives that the maximum voltages across diodes D_1, D_2 are 220 V, which is about $V_o/2$, and the maximum voltages across diodes D_3 and D_4 are 110 V, which is about $V_o/4$. It means that all of the diodes D_1, D_2, D_3 and D_4 have low voltage stress.

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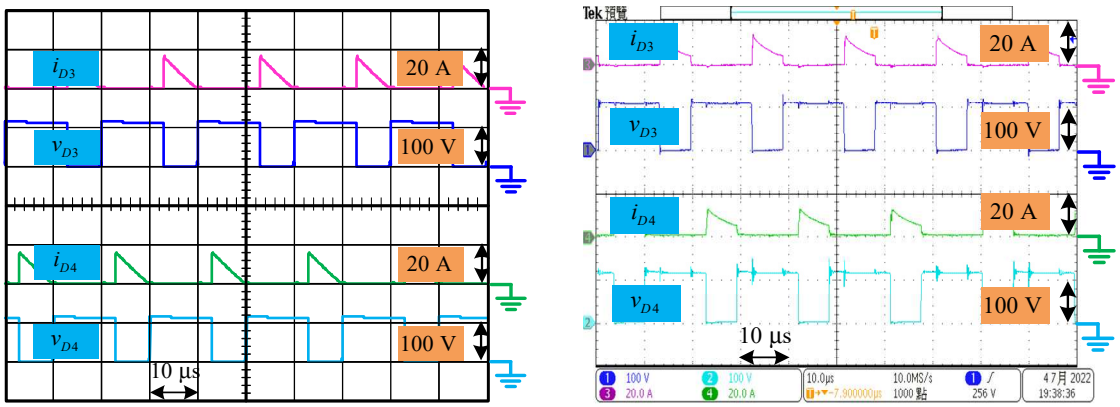

(a) (b)

Figure 13. Waveforms for i_{D3}, v_{D3}, i_{D4} and v_{D4}.: (**a**) Simulation results (**b**) Experimental results.

Figure 14 shows the dynamic response for the output voltage when there is a step change in the output load from 200 W to 1000 W and then to 200 W. It has a voltage overshoot of 2.3 V, which is much less than the output voltage of 400 V. Figure 15 shows the dynamic response for the output voltage when there is a step change in the input voltage from 40 V to 36 V and then to 40 V. The output voltage overshoot is 0.71 V, which is quite smaller than the output voltage of 400 V. The results in these two figures show that the output voltage can be regulated under input voltage and output load variations. It means that the overall system is very robust.

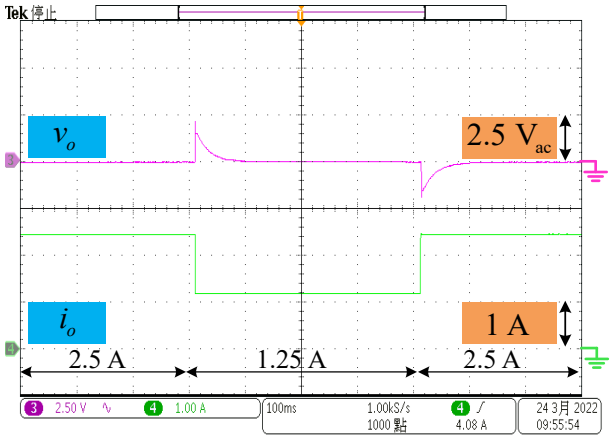

Figure 14. Dynamic response for output voltage for a step change in load (200 W -1000 W -200 W).

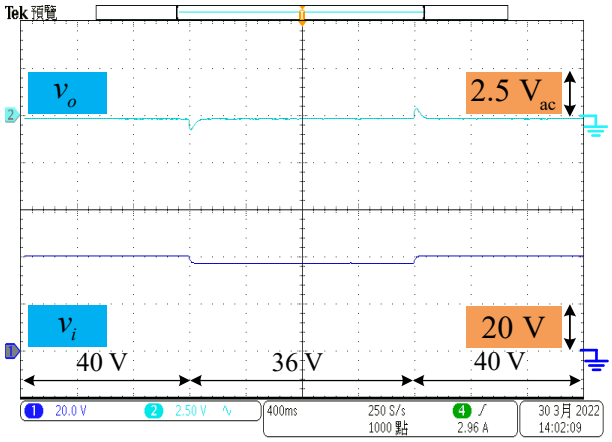

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Figure 15. Dynamic response for output voltage for a change in input voltage (40 V -36 V -40 V).

In this paper, the conversion efficiency of the proposed converter for output powers from 200 W to 1000 W was measured by a HIOKI 3390 and the results are shown in Figure 16. The converter has a maximum efficiency of 95.5 % at a light load of 200 W. A heavy load of 1000 W results in the efficiency of 91.16 %, which is still more than 90 %. Moreover, the picture of the experimental prototype for power stage is also presented in Figure 17. It shows that the proposed converter has a simple circuit structure with fewer components.

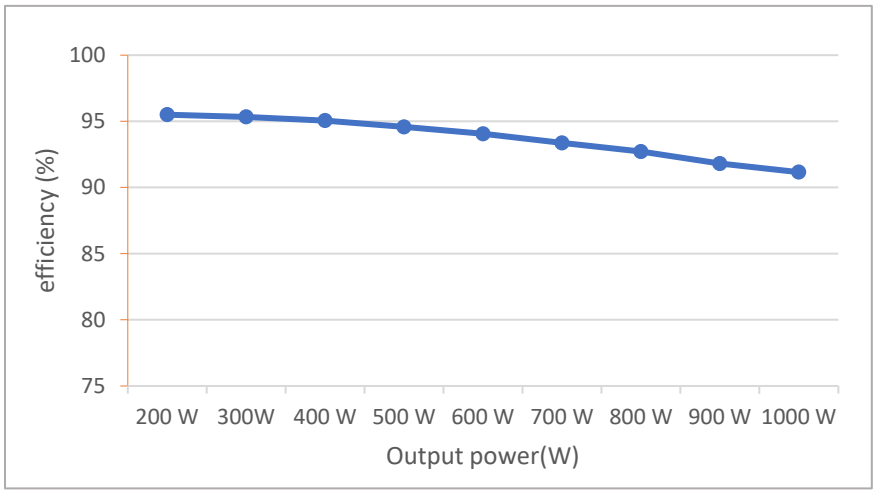

Figure 16. Measured efficiency of the proposed converter.

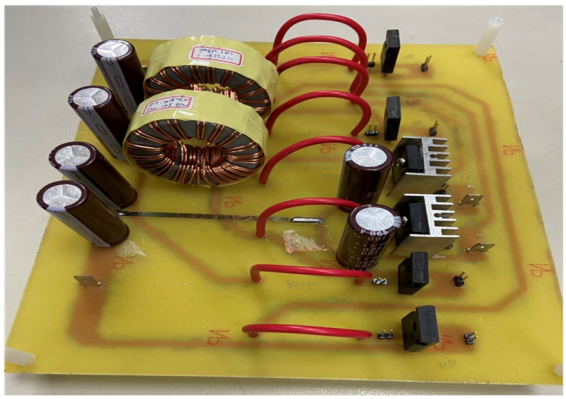

Figure 17. Experimental prototype for power stage.

6. Conclusion

This paper proposes a novel symmetrical active-switched coupled-inductor high-step-up DC/DC converter. The new active-switched coupled-inductor boost technology features both switching inductor and coupled inductor boost characteristics so the converter can be easier to achieve a higher voltage gain with two design freedom of the turn ratio and the duty cycle and operated without a large duty cycle. Moreover, the voltage stresses on the switches and diodes in the converter are much lower than the output voltage. It gives that the power switches with a smaller ON-resistance and diodes with smaller forward voltage can applied to reduce conduction losses. So the overall efficiency of the proposed converter can be further increased. A steady-state analysis, component design considerations, dynamics and controller design are also presented herein. Finally, a 200-1000 W with 40 V input and 400 V output at 50 kHz switching frequency prototype is implemented. The simulations and experimental results are thereby given to validate the theoretic

results. It reveals that the proposed converter exhibits a high voltage gain of 10, low voltage stresses of power switches and diodes, output voltage regulation despite of input voltage and output load variations, and high efficiency of 95.5 % at 200 W. As a result, the proposed converter with high voltage gain, low voltage stress, high efficiency and simple circuit topology can be used for a rectifier giving a 400 V dc bus in a renewable energy generation system.

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