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[Zhuofan Wang](#) , Hongliang Lu , [Yuming Zhang](#) , [Chen Liu](#) *

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Article

Ultrathin Encapsulation Strategies with Predefined Gate Dielectric Surface Area for Flexible Crystalline Silicon Nanomembrane Based MOS Capacitors

Zhuofan Wang, Hongliang Lu, Yuming Zhang and Chen Liu *

Key Laboratory for Wide Band Gap Semiconductor Materials and Devices of Education Ministry, School of Microelectronics, Xidian University, Xi'an 710071, China; zhuofanxidian@sina.com (Z.W.); hllv@mail.xidian.edu (H.L.); zhangym@xidian.edu.cn (Y.Z.)

* Correspondence: liuchen@xidian.edu.cn

Abstract: Crystalline silicon nanomembrane (Si NM) is promising in wearable and implantable bioelectronics due to its electrical and mechanical performances. However, the current explorations are not enough to firmly bridge ultrathin encapsulation strategies with high performance crystalline Si NM based transistors. In this work, we utilized Al₂O₃/alucone as the ultrathin encapsulation strategies aim to thoroughly investigate the effect of gate dielectric surface area on the electrical performance of crystalline Si NM based metal-oxide-semiconductor capacitors (MOSCAPs). The comparative analysis was implemented on the three types of diameters (\varnothing) MOSCAPs with and without Al₂O₃/alucone encapsulation under planar and concave/convex bending conditions. Benefited from the Al₂O₃/alucone ultrathin encapsulations, the stability of gate leakage current density, and interfacial characteristics were maintained and improved under mechanical bending deformations for MOSCAPs with predefined \varnothing of 160, 240, and 320 μm compared to the bare MOSCAPs. Combined with the \varnothing -related mechanical analysis on the maximum strain in the critical layers and the practical measurements, the encapsulated MOSCAPs with \varnothing 160 μm showed the most stable electro-mechanical performances. The variations for encapsulated MOSCAPs with three types of \varnothing emerged in the oxide layer and the interface at dielectric/Si NM that were carefully evaluated according to the bending deformations. These findings are significant for leveraging the practical applications in the ultrathin encapsulation strategies for reliable operations of crystalline Si NM based integrated circuits (ICs).

Keywords: ultrathin encapsulation; silicon nanomembrane; metal-oxide-semiconductor capacitors; gate dielectric surface area

1. Introduction

Thin film encapsulation is indispensable in the prevailing Internet of Things (IoT) due to its practical applications in biomedical engineering, precision medicine, and brain-computer interfaces [1, 2]. Considerable efforts have been made to improve the lifetime of wearable and implantable devices such as thin film electrodes [3], field-effect transistors (FETs) [4], and organic electrochemical transistors (OECTs) [5]. Taking advantage of high performances, high areal density, and low cost, crystalline silicon nanomembrane (Si NM) shows excellent mechanical and electrical properties as active electrodes recording the signals from the human body through advanced complementary metal-oxide-semiconductor (CMOS) techniques, which has huge potential for medical bioelectronics [6, 7]. To achieve long-term reliable operation for crystalline Si NM based CMOS devices, it is urging to use optimized thin film encapsulation strategies for maintaining durability in curvilinear, soft, and wet environments. Benefiting from the advancements in techniques of atomic layer deposition (ALD) and molecular layer deposition (MLD), the conformality, scalability, and CMOS compatibility for thin film encapsulation have been promoted and the ultrathin encapsulation strategies have started to attract more attention [8, 9]. To function, gate dielectric surface area is the primary factor to be considered for the designs in ultrathin encapsulation strategies of crystalline Si NM based metal-oxide-semiconductor field-effect transistors (MOSFETs). Because the size of gate films and dielectric

island substantially affected the capacitive coupling between the tissue and flexible electronics encapsulated by ultrathin encapsulation, especially varied the gate controls in CMOS devices with the top gate top contact configuration. However, the investigations into the effect of different gate dielectric surface areas on the crystalline Si NM based CMOS devices with ultrathin encapsulation strategies, have yet to be revealed.

For ultrathin encapsulation strategies, the researchers made considerable efforts on the physically transferred ultrathin membranes with submicrometre thickness [10], hybrid inorganic/organic films [11], and mechanical strain optimizations [12]. The representative work on physically ultrathin membranes is delivering SiO₂ thermally grown on rigid Si wafers and transferring it on crystalline Si NM based transistors to serve as barrier films and the capacitive interface to the tissues leading to the multidecade lifetimes on timescales [13, 14]. Recently, the insertion of alucone organic layer into the atomic layer deposited Al₂O₃ inorganic layer showed promising results on the barrier performance and transmittance better than the single layer of Al₂O₃ [15]. Due to the Al₂O₃/alucone composites, the mechanical stability of Ag nanowire electrodes was largely improved by monitoring the electrical resistance in over 300,000 cycles of bending tests [16]. For mechanical strain optimizations, thin film encapsulation is an effective way to release the external strain in the device layer by optimizing the locations of neutral mechanical planes (NMP) towards the encapsulation layer [17, 18]. As the thickness of the encapsulation layer decreases from the micrometer scale to the nanometer scale, it is more important to thoroughly consider the effect of gate dielectric surface area as the form factor on the ultrathin encapsulation strategies in crystalline Si NM based transistors.

In this work, we investigated the effect of gate dielectric surface area on the electrical properties of crystalline Si NM based metal-oxide-semiconductor capacitors (MOSCAPs) in ultrathin encapsulation strategies of Al₂O₃/alucone nanolaminates under planar and concave/convex bending conditions. Section 2 revealed the effect of Al₂O₃/alucone nanolaminates and different gate dielectric surface areas on the maximum strain in the MOSCAPs' device layer changed as a function of bending radii. In section 3, the basic electrical properties of encapsulated and bare MOSCAPs were analyzed as changes in gate dielectric surface areas under a planar state. Importantly, Section 4 comparatively depicted electrical parameters reflecting the variations of oxide layers and interfacial properties for encapsulated and bare MOSCAPs with different sizes of dielectric islands under concave and convex bending conditions. Finally, conclusions were delivered in Section 5.

2. Maximum strain analysis in the device layer for Al₂O₃/alucone encapsulated and bare MOSCAPs with different \varnothing

Figure 1 explicitly illustrates the cross-sectional view of MOSCAPs with (w/) and without (w/o) 3.5 dyads (one Al₂O₃ layer and one alucone layer) Al₂O₃/alucone encapsulation owing to the multilayered structures were defined as composite beams. Notably, the width of encapsulation layers includes two parts (i.e., W_{1_encap} and W_{2_encap}) with specifications as follows: (1) alternated 11 nm Al₂O₃ and 3.5 nm alucone to generate 3.5 dyads nanolaminates on the anode metal of circular MOSCAPs through atomic/molecular layer deposition (ALD/MLD). (2) the total thickness of the ultrathin encapsulation layer (54.5 nm) is less than the thickness of anode metal film (180 nm). W denotes the width of the beam, W_{gate} denotes the width of the anode (i.e., the \varnothing of the anode), W_{1_encap} is equal to W_{gate} , and W_{2_encap} is equal to $(W - W_{gate})/2$. From the layout design, W is 500 μm and W_{gate} is defined as three types of 160 μm , 240 μm , and 320 μm . The mechanical performances of Al₂O₃/alucone encapsulated and bare MOSCAPs in configurations of different anode diameters (\varnothing) under extreme bending conditions are comparatively investigated using mathematical models. The neutral mechanical plane (NMP) conceptually represents the surface in the beam where the bending stress is zero. The W_{gate} related location of the NMP in encapsulated and bare MOSCAPs and the corresponding strain in the multilayered structures are given by [19]

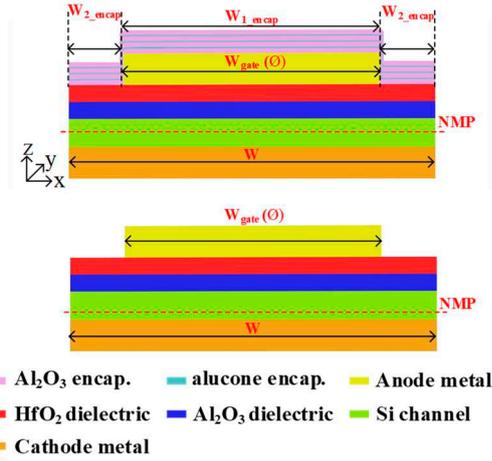


Figure 1. Cross-sectional schematic illustration of Al₂O₃/alucone encapsulated (upper) and bare (lower) MOSCAPs labeled with width dimensions and NMP positions.

$$\left\{ \begin{array}{l} z_0 = \frac{\sum_{i=1}^N \bar{E}_i A_i \left[\left(\sum_{j=1}^i h_j \right) - \frac{h_i}{2} \right]}{\sum_{i=1}^N \bar{E}_i A_i} \\ \varepsilon = \frac{z - z_0}{R} \end{array} \right. \quad (1)$$

where z_0 is the distance from NMP to the bottom surface of the composite beam, N is the total layers, A_i is the cross-sectional area for every investigated layer, \bar{E}_i and h_i respectively represent the plane-strain modulus and thickness for i^{th} layer. \bar{E}_i is calculated by $E_i/(1-\nu^2)$, ε is the strain in the beam, R is the bending radius, and z is the distance from the position of interest to the bottom surface. Specifically, for encapsulated MOSCAPs with different \varnothing of 160 μm , 240 μm , and 320 μm the distance from NMP to the bottom surface of the Si channel layer is 101.13 nm, 110.87 nm, and 119.7 nm. For bare MOSCAPs with \varnothing of 160 μm , 240 μm , and 320 μm the distance from NMP to the bottom surface of the Si channel layer is 55.96 nm, 69.53 nm, and 81.67 nm. As for the original state in encapsulated MOSCAPs with \varnothing of 160 μm , the NMP position is moved towards the mid-surface of the Si channel compared to the bare MOSCAPs. Afterward, the location of NMP further rises in encapsulated and bare MOSCAPs as the \varnothing increases to 240 μm and 320 μm . This phenomenon leads to the difference of applied strain in the device layer varying with R , as plotted in Figure 2.

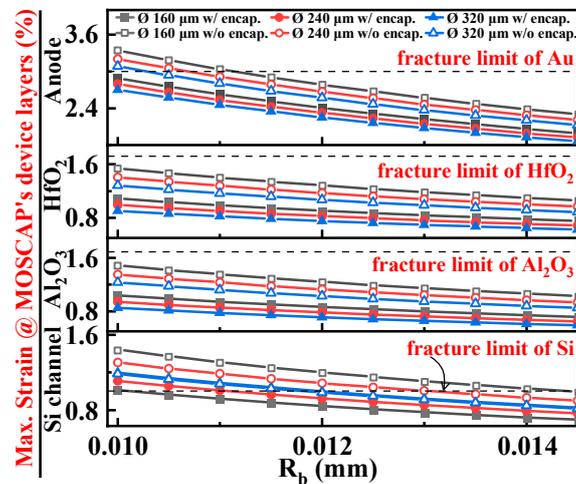


Figure 2. Maximum strain in the device layer, i.e., anode, HfO₂/Al₂O₃ bilayered dielectric, and Si channel layer, changed as bending radii (R_b) for Al₂O₃/alucone encapsulated and bare MOSCAPs with different diameters (Ø).

It is important to explore the strain in flexible multi-layered devices, especially under extreme bending conditions to understand the effect of encapsulation layer on MOSCAPs with different Ø. In general, the applied strain versus R curve is monotonically decreased in the order of increasing Ø for encapsulated and bare MOSCAPs in the anode layer and dielectric bilayers. The difference occurs in the Si channel layer of encapsulated MOSCAPs, i.e., the applied strain employed by increasing Ø exhibits a positive correlation on strain versus R curves. The main cause is attributed to the maximum strain in encapsulated MOSCAPs with Ø of 240 µm and 320 µm appearing at the bottom surface of the Si channel which the distance between NMP and calculated position is larger than the related distance in the device with Ø 160 µm. Moreover, the strain of fracture limit is represented by the black dashed line in Figure 2 for every critical layer highlighting the huge difference between Al₂O₃/alucone encapsulated and bare MOSCAPs that are equipped with different Ø. At the anode metal layer, the applied strain at R=11 µm for bare MOSCAPs with Ø 160 µm reaches the fracture limit of Au (i.e., 3 %). However, the applied strain could be kept below 3 % even at R=10 µm for encapsulated MOSCAPs with the same Ø. As the Ø increase to 240 µm and 320 µm, the applied strain is further less than 3 % for encapsulated MOSCAPs, but for bare MOSCAPs, the applied strain at 240 µm and 320 µm maintain exceeding 3 % at R=10 µm.

At the HfO₂ and Al₂O₃ dielectric layer, the strain versus R relation for the bare MOSCAPs with Ø 160 µm takes the leading increase approaching the strain of fracture limit (i.e., 1.72 % for HfO₂ and 1.69 % for Al₂O₃). Importantly, it can be concluded that the variations of maximum strain at bilayered dielectric layer decrease 0.45 %, 0.41 %, and 0.38 % for encapsulated MOSCAPs with Ø 160 µm, 240 µm, and 320 µm, in comparison to bare MOSCAPs. Compared to the other four curves, the strain versus R curves at the Si channel reflect unique and favorable behavior for encapsulated MOSCAPs with Ø 160 µm. The applied strain is kept beneath the strain of fracture limit in the Si channel (i.e., 1 %) because the optimized NMP for Al₂O₃/alucone encapsulated MOSCAPs in the configuration of Ø 160 µm is almost located at the mid-surface of the Si channel. Thus, these calculations prove that the Ø as form factors are substantially affecting the bending radii related mechanisms for Al₂O₃/alucone encapsulated and bare MOSCAPs. It emphasizes that the NMP optimization towards the critical layer in MOSCAPs with ultrathin encapsulation should be carefully designed for the ultrathin Si channel-based devices. The mechanical parameters for each layer in numerical analysis are summarized in the **Appendix**.

3. C-V and J-V characteristics at the planar state for encapsulated and bare MOSCAPs with different Ø

To explore the gate dielectric surface areas related mechanisms under bending conditions for MOSCAPs in the configuration of ultrathin encapsulation strategies, we fabricated monocrystalline Si NM based MOSCAPs on plastic substrates with encapsulation structure of ultrathin Al₂O₃/alucone nanolaminates. The predefined gate surface area of circular MOSCAPs is 0.02 mm², 0.05 mm², and 0.08 mm² according to the Ø of 160 µm, 240 µm, and 320 µm. To begin with, the electrical measurements at the planar state were thoroughly employed on samples of encapsulated and bare MOSCAPs with various Ø. The Inset of Figure 3 schematically demonstrates a multi-layered structure for devices under flat conditions, namely 3.5 dyads Al₂O₃/alucone nanolaminates as encapsulation layer deposited on the circular MOSCAPs. Figure 3 depicts the measured capacitance versus voltage curves at 100 kHz when the voltage swept from -2 V to +2 V for different Ø of circular MOSCAPs w/ and w/o Al₂O₃/alucone encapsulation. The consistency of results is confirmed by 30 devices. Even though the values have a slight difference the tendency is still steady. As for circular MOSCAPs with three types of Ø, the representative results are summarized in Figure 3, clarifying three viewpoints. Firstly, the MOSCAPs clearly distinguish from depletion to inversion until the maximum capacitance of encapsulated and bare devices reaches 0.27 to 0.28 µF/cm² consistently.

Secondly, it is obvious that the flatband voltage (V_{fb}) negatively shifts in bare and encapsulated MOSCAPs with different \varnothing from 160 μm to 320 μm . This phenomenon is due to both the operational point of MOSCAPs and the amounts of charges in the oxide layer being controlled by different gate dielectric surface areas. Thirdly, compared to the bare MOSCAPs with the same \varnothing , $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulated devices maintain a similar slope indicating the presence of ultrathin encapsulation nanolaminates ensures the stability in interfacial characteristics at the planar state. Figure 4 depicts the current density versus voltage (J-V) curves change as a function of \varnothing for encapsulated and bare MOSCAPs. Notably, the current density decreased with the increase in \varnothing of circular MOSCAPs. Specifically, the gate leakage current density (J_g) is effective in valuing ultrathin dielectric islands in encapsulated Si NM based MOSCAPs with different \varnothing . At the planar state, J_g at 0.5 V for encapsulated circular MOSCAPs with \varnothing of 160 μm , 240 μm , and 320 μm are 3.95×10^{-9} A/cm², 3.48×10^{-9} A/cm², and 2.61×10^{-9} A/cm². Yet the J_g synchronously increased to 5.22×10^{-9} A/cm², 5.11×10^{-9} A/cm², and 3.30×10^{-9} A/cm² for bare MOSCAPs with same \varnothing . It can be concluded from the C-V and J-V results for encapsulated and bare MOSCAPs that at the planar state, the \varnothing of circular MOSCAPs varied from 160 μm to 320 μm facilitating the more negative shift V_{fb} accompanied by decreased J_g . Overall, the investigation of electrical properties is worth further exploring the effect of different \varnothing on circular MOSCAPs w/ and w/o ultrathin encapsulation under bending deformations.

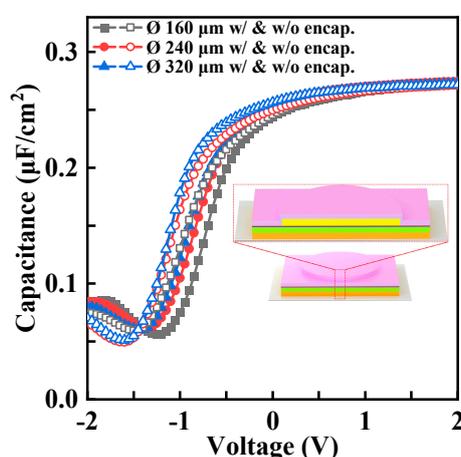


Figure 3. C-V curves at the planar state obtained from encapsulated and bare MOSCAPs with different \varnothing . Inset: schematic illustration of encapsulated MOSCAPs on the bendable substrate.

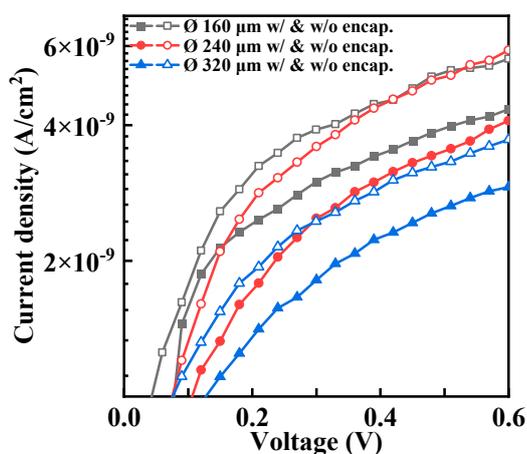


Figure 4. J-V curves at the planar state obtained from encapsulated and bare MOSCAPs with different \varnothing .

4. Electro-mechanical analysis under bending conditions for encapsulated and bare MOSCAPs with different \varnothing

4.1. Comparative analysis on basic electrical properties

Bending tests were thoroughly implemented on circular MOSCAPs with three types of \emptyset simultaneously for the encapsulated and bare flexible devices. The flat state denotes that the bending radius is infinite. The concave and convex bending states denote bent at a defined radius inwardly and outwardly as schematically illustrated in the inset of Figure 5. Based on the previous investigation on MOSCAPs using flexible monocrystalline Si NM, the bending radii carefully adopted the concave bending radii of 110.5 mm and 85 mm (i.e., (-)110.5 mm and (-)85 mm), as well as the convex bending radii of 77.5 mm and 38.5 mm (i.e., (+)77.5 mm and (+)38.5 mm). Figure 5 depicts the dynamic changes on C-V curves under bending deformations for \emptyset 160 μm circular MOSCAPs w/ and w/o ultrathin $\text{Al}_2\text{O}_3/\text{alucone}$ nanolaminates. For comparison, The C-V results influenced by bending radii for $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulated and bare circular MOSCAPs with \emptyset of 240 μm and 320 μm are shown in Figure 6 and Figure 7, respectively. Figure 8 depicts the comparative analysis of maximum capacitance (C_{max}) with different \emptyset for encapsulated and bare MOSCAPs. The changes in C_{max} of encapsulated MOSCAPs with three types of \emptyset are varied from -3.5 % to +2.7 % at concave bending radii of (-)110.5 mm and (-)85 mm. The changes in C_{max} of encapsulated MOSCAPs with \emptyset 160 μm and \emptyset 240 μm are varied from -0.5 % to +0.9 % at convex bending radii of (+)77.5 mm and (+)38.5 mm. However, a significant reduction of C_{max} appeared in encapsulated MOSCAPs with \emptyset 320 μm at convex bending radii, namely -16.5 % at (+)77.5 mm and -20.5 % at (+)38.5 mm. According to the applied voltage, the obvious "stretch-out" phenomenon occurred at encapsulated MOSCAPs with \emptyset 320 μm , which denotes the presence of interface states and changes as the different bending conditions. Compared to the encapsulated MOSCAPs, the C_{max} in bare MOSCAPs behaved undesirably at the smallest and largest \emptyset . A relatively large reduction in C_{max} of \emptyset 160 μm and \emptyset 320 μm with -2 % and -7.9 % at high concave bending deformation of 85 mm, when the variations reached -3.6 % and -26.3 % at high convex bending deformation of 38.5 mm. At \emptyset of 240 μm , the C_{max} of bare MOSCAPs is relatively stable with variations ranging from -1.9 % to +1.8 % at four bending radii. In addition, it is observed that V_{fb} of bare devices with \emptyset of 160, 240 and 320 μm shifted positively as a function of bending radii. These observations on C-V results illustrate that the $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulated MOSCAPs with \emptyset of 160, 240, and 320 μm can effectively promote the stability of C_{max} under bending deformations, compared to the same \emptyset of bare devices. However, the \emptyset related mechanisms for $\text{Al}_2\text{O}_3/\text{alucone}$ -encapsulated and bare MOSCAPs are not monotonically changed with the increase of \emptyset thus it is supposed to be discussed in a multi-dimensional such as the reliability of the dielectric layer and interface at dielectric/Si NM.

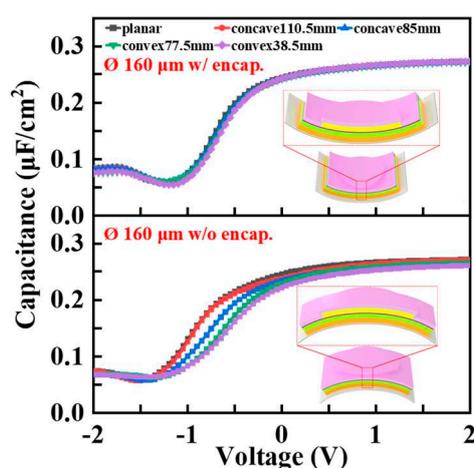


Figure 5. C-V curves of MOSCAPs with \emptyset 160 μm under bending conditions. Inset: schematic illustration of encapsulated MOSCAPs bent inwardly and outwardly.

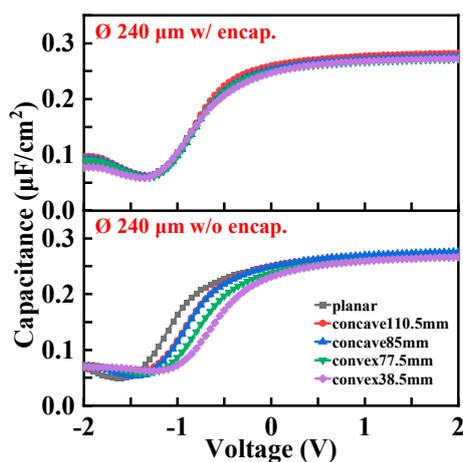


Figure 6. C-V curves of circular MOSCAPs with $\text{Ø } 240 \mu\text{m}$ under bending conditions.

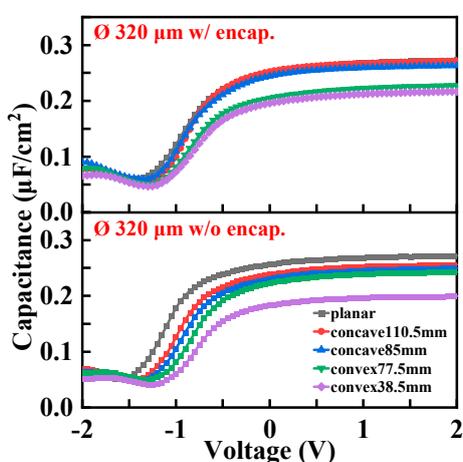


Figure 7. C-V curves of circular MOSCAPs with $\text{Ø } 320 \mu\text{m}$ under bending conditions.

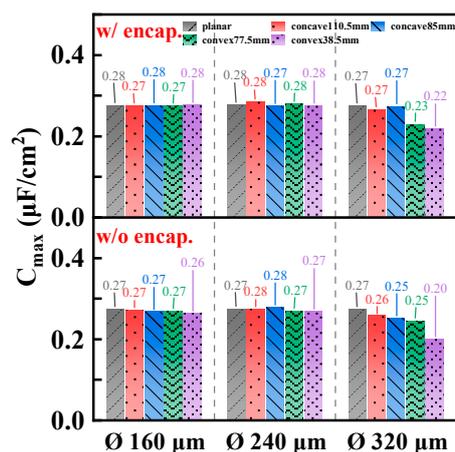


Figure 8. The maximum capacitance (C_{max}) changed as a function of Ø under bending conditions.

Figure 9 comparatively illustrates the J-V curves of circular MOSCAPs w/ and w/o $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulation under bending deformations that changed with three types of Ø at $160 \mu\text{m}$, $240 \mu\text{m}$, and $320 \mu\text{m}$. As the increase of bending deformations, the J-V curves gradually rose for encapsulated and bare MOSCAPs with three predefined gate surface areas. It is noticeable from the J-V characteristics that the performance of $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulated MOSCAPs with $\text{Ø } 320 \mu\text{m}$ is most favorable under bending deformations compared to the other two. Importantly, the J_g values were

analyzed to investigate the stability of gate dielectric manipulated by both bending radii and gate surface area, as shown in Figure 10. Compared to the planar state, the variations on J_g at 0.5 V of encapsulated MOSCAPs with \varnothing 240 μm increased to 1.07, 1.17, 1.24, and 1.24 times at four bending radii, whereas it increased to 1.05, 1.37, 1.75, and 1.82 times in bare MOSCAPs with \varnothing 240 μm corresponding to the same bending deformation. It denotes that the \varnothing 240 μm of encapsulated MOSCAPs is reliable to inhibit the growth of J_g in bare MOSCAPs under bending deformations. Followed by the variations on J_g for \varnothing 320 μm increased to 1.01, 1.04, 1.07, and 1.13 times in encapsulated devices while increased to 1.13, 1.23, 1.34, and 1.51 times in bare devices under four bending conditions when compared with the planar state. Although the variations on J_g are also inhibited by encapsulated MOSCAPs with \varnothing 160 μm , the magnitude of the difference is inferior to the \varnothing 240 μm and \varnothing 320 μm of encapsulated devices. Hence, the J-V results under bending deformations indicate that the $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulated MOSCAPs with \varnothing 320 μm and \varnothing 240 μm take the leading role in both stabilizing J_g and relieving the increase of J_g under bending deformations when compared to the bare MOSCAPs.

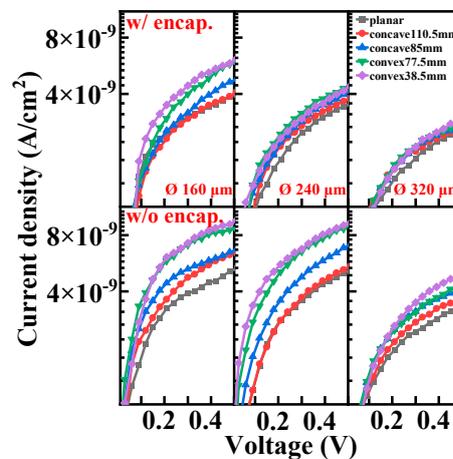


Figure 9. J-V curves changed as a function of \varnothing under bending conditions.

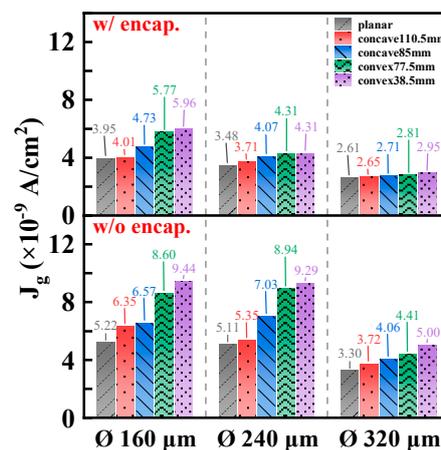


Figure 10. The gate leakage current density (J_g) changed as a function of \varnothing under bending conditions.

4.2. Comparative analysis on extracted parameters

The variations on V_{fb} for encapsulated and bare MOSCAPs are positively shifted with the increase of bending deformations under concave and convex conditions, as mentioned in Section 4.1. It may be attributed to that the more electrons are injected by increasing mechanical strains but the behavior of fluctuated magnitude of V_{fb} from planar to bent state is varied with \emptyset for MOSCAPs w/ and w/o encapsulation. It is significant to compare the V_{fb} and effective oxide charge (N_{eff}) in encapsulated and bare MOSCAPs. The V_{fb} corresponding to C_{fb} is extracted from C-V curves, C_{fb} and N_{eff} are calculated as follows [20]:

$$\begin{cases} C_{fb} = \frac{C_{max}}{1 + \frac{(C_{max}/C_{min}) - 1}{2\sqrt{\ln(|N_A - N_D|/n_i)}}} \\ N_{eff} = \frac{C_{max} \times \Delta V_{fb}}{q \times A} \end{cases} \quad (2)$$

where C_{max} and C_{min} are the maximum and minimum capacitance of measured C-V curves, N_A is the acceptor concentration, N_D is the donor concentration, n_i is the intrinsic carrier concentration, ΔV_{fb} is the theoretical V_{fb} minus extracted V_{fb} , q is the electron charge, and A is the gate surface area of MOSCAPs. Figure 11 summarizes the V_{fb} and N_{eff} for encapsulated and bare MOSCAPs with \emptyset from 160 μm to 320 μm under bending conditions. Compared to the encapsulated devices with \emptyset 160 μm and \emptyset 320 μm , the encapsulated MOSCAP of \emptyset 240 μm presents the most desirable ability to alleviate the instability of V_{fb} in bare devices. Specifically, the precise variations that V_{fb} at four bending radii of (-)110.5 mm, (-)85 mm, (+)77.5 mm, and (+)38.5 mm minus V_{fb} at planar state (i.e., $V_{fb} - V_{fb,o}$), which are extracted as small as 0.005 V, 0.034 V, 0.009 V, and 0.023 V. It manifests that encapsulated MOSCAPs with \emptyset 240 μm is beneficial to relieve the strain in gate dielectric layer leading to the enhancement of stability on J_g and V_{fb} . At the planar state, the N_{eff} in encapsulated MOSCAPs with \emptyset of 160 μm , 240 μm , and 320 μm is $4.14 \times 10^{11} \text{ cm}^{-2}$, $5.74 \times 10^{11} \text{ cm}^{-2}$, and $6.99 \times 10^{11} \text{ cm}^{-2}$. The N_{eff} increased to $7.0 \times 10^{11} \text{ cm}^{-2}$, $10.61 \times 10^{11} \text{ cm}^{-2}$, and $11.38 \times 10^{11} \text{ cm}^{-2}$ for bare MOSCAPs with \emptyset of 160 μm , 240 μm , and 320 μm . However, as the applied bending deformations, the decrease of N_{eff} is obvious in the bare MOSCAPs, probably because the physical thickness of the gate dielectric layer with larger size is more sensitive to being altered and affected by bending strains without the protection of ultrathin encapsulation layer.

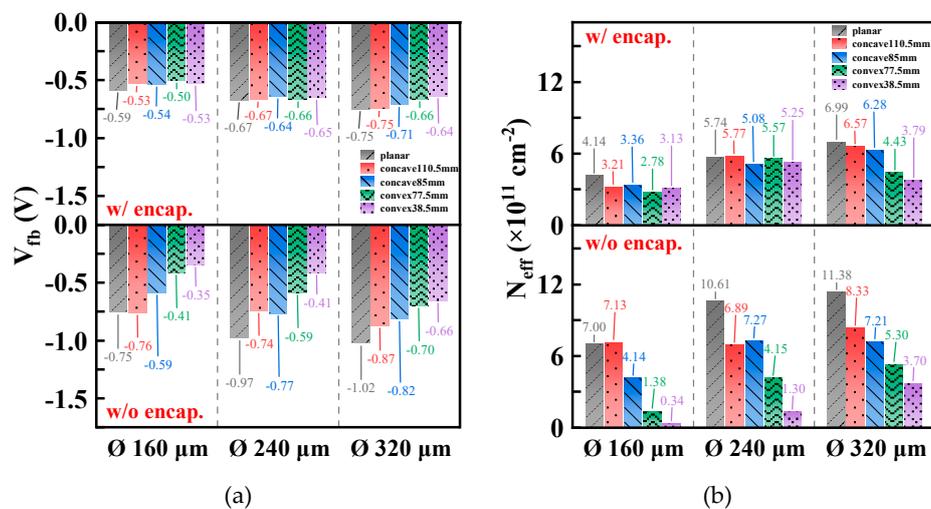


Figure 11. (a) V_{fb} and (b) N_{eff} changed as a function of \emptyset in MOSCAPs w/ and w/o encapsulation under bending conditions.

Figure 12 illustrates the C_{\max} divided by C_{\max} at 1 kHz (i.e., normalized $C_{\max}(\omega)$) changed with \emptyset of 160 μm , 240 μm , and 320 μm in encapsulated and bare MOSCAPs. Figure 13 illustrates the extracted values of frequency dispersion according to the varied \emptyset under bending conditions. Notably, the frequency dispersion from \emptyset 160 μm to \emptyset 320 μm is 9.19 %/Dec, 7.67 %/Dec, and 8.3 %/Dec at the planar state for bare MOSCAPs, which is relatively large and fluctuating. But the frequency dispersion at the planar state is extremely stable for encapsulated MOSCAPs from \emptyset 160 μm to \emptyset 320 μm , which is 6.29 %/Dec, 6.63 %/Dec, and 6.68 %/Dec. Among three types of \emptyset in encapsulated MOSCAPs, \emptyset 160 μm maximally maintains stability on frequency dispersion under four bending conditions but the larger areas of \emptyset 240 μm and \emptyset 320 μm only performed better under concave bending conditions than convex. The C_{\max} performances for encapsulated MOSCAPs with \emptyset 320 μm under concave and convex bending deformations are consistent with the properties of the frequency dispersion. While the increased frequency dispersion for encapsulated MOSCAPs with \emptyset 240 μm denotes the substantial changes in interface states. In addition, compared to \emptyset 160 μm and \emptyset 320 μm , the frequency dispersion of bare MOSCAPs with \emptyset 240 μm is most stable under bending deformations which is due to the robustness of both C_{\max} and interfacial properties. Hence, the results of frequency dispersion denote that the smallest \emptyset of 160 μm is the favorable choice in the ultrathin encapsulation strategies, but it needs optimizations on the strain insensitivity of both the ultrathin dielectric layer and interface between dielectric and ultrathin channel as \emptyset increases.

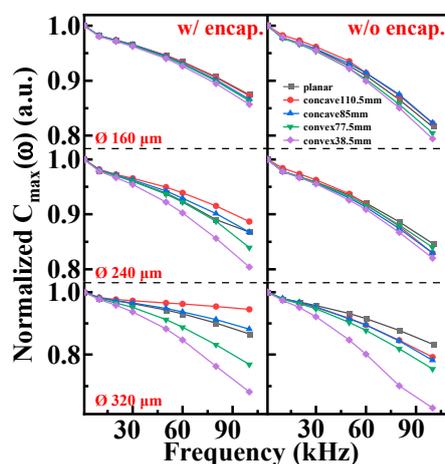


Figure 12. Normalized C_{\max} versus frequency (ω) for encapsulated and bare MOSCAPs with three types of \emptyset .

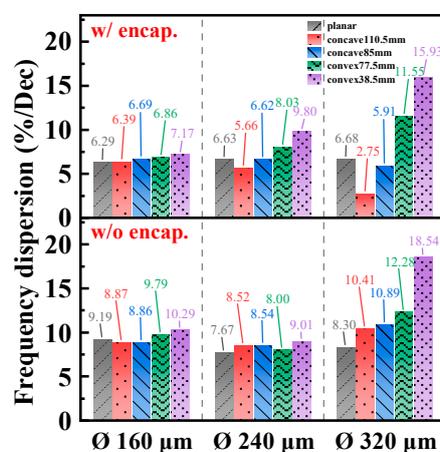


Figure 13. Frequency dispersion in percentages per decade changed as a function of \emptyset under bending conditions.

4.3. Comparative analysis on interfacial characteristics

Figure 14a illustrates the D_{it} distribution for $\text{Al}_2\text{O}_3/\text{alucone}$ encapsulated and bare MOSCAPs with \varnothing 160 μm under bending conditions. The D_{it} values were extracted by Terman methods [21]. The encapsulated MOSCAPs with \varnothing 160 μm exhibit almost similar changes in bending strains related to D_{it} distribution compared to the bare device with the same \varnothing of 160 μm , which is probably due to the optimized NMP position in the Si channel using ultrathin encapsulation strategies. When the \varnothing increased, the variations in D_{it} distribution differed at 240 μm and 320 μm , as shown in Figures 14b and 14c. For \varnothing 240 μm of encapsulated and bare MOSCAPs, the obvious increase in D_{it} according to bending strains is verified in the former. Yet, the relatively stable performance in the latter is due to the reliability of both C_{max} and frequency dispersion. When the \varnothing further increased to 320 μm for bare MOSCAPs, the D_{it} values at investigated E_c - E entirely increased two orders of magnitude under high deformation of (+)38.5 mm. Hence, the encapsulated MOSCAPs with \varnothing 320 μm can maintain the stability of D_{it} distributions under bending conditions. Moreover, in encapsulated MOSCAPs with \varnothing 320 μm , D_{it} values distributed at 0.33 eV beneath the conduction band (E_c) at bending states notably increased to 2 times at the planar state.

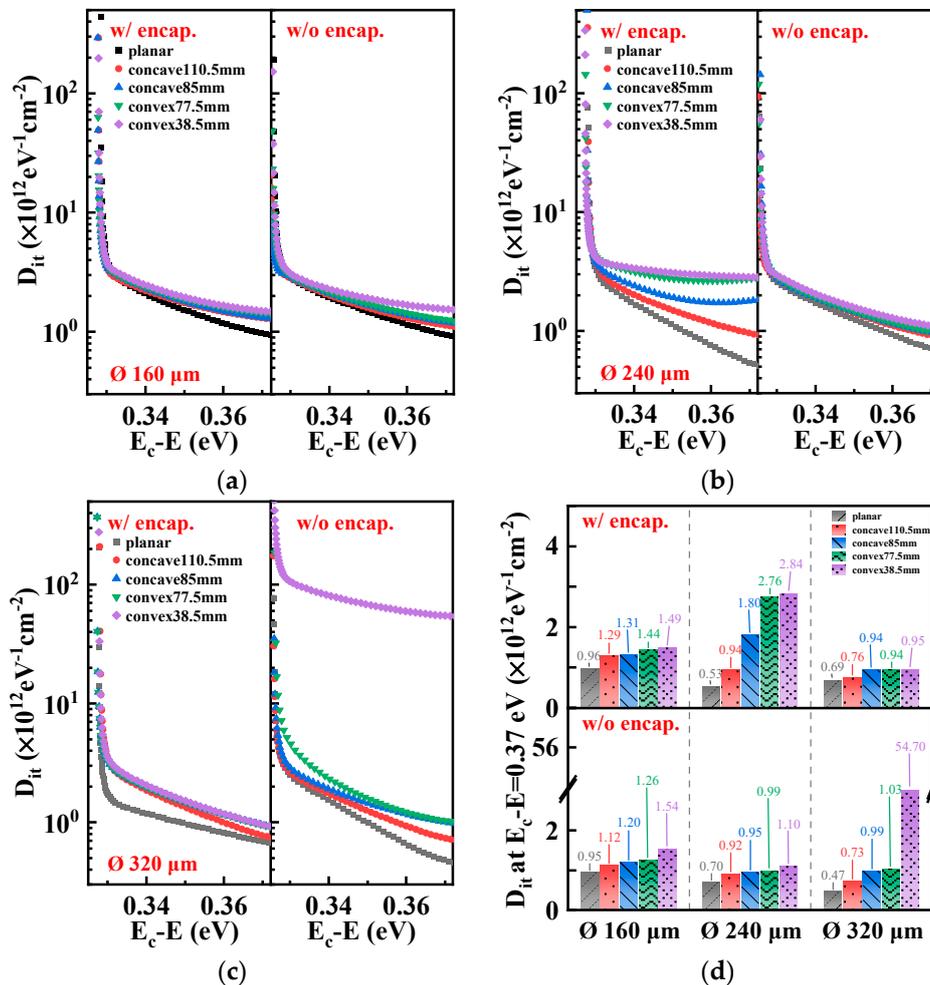


Figure 14. Interface trap density (D_{it}) distribution changed with the energy level of E_c-E under bending conditions for encapsulated and bare MOSCAPs with \varnothing of (a) 160 μm , (b) 240 μm , and (c) 320 μm . (d) D_{it} corresponds to E_c-E at 0.37 eV changed as a function of \varnothing under bending conditions.

Importantly, the D_{it} values for encapsulated and bare MOSCAPs with three types of \varnothing are representative at the energy level of $E_c-E = 0.37$ eV (i.e., 0.19 eV above midgap) that changed with different \varnothing under bending deformations, as shown in Figure 14(d). Compared to the planar state, the variations on D_{it} at the energy level of $E_c-E = 0.37$ eV of MOSCAPs with \varnothing 160 μm increased to 1.3, 1.4, 1.5, and 1.6 times in encapsulated devices at four bending radii. Yet, it increased to 1.2, 1.3, 1.3,

and 1.6 times in bare devices corresponding to the same bending deformation. The variations are continually stable for larger \varnothing of 240 μm in bare MOSCAPs which increased to 1.3, 1.4, 1.4, and 1.6 times. But the values rose rapidly for the largest \varnothing of 320 μm in bare MOSCAPs which increased to 1.6, 2.1, 2.2, and 116.2 times under four bending conditions compared with the planar state. On the other hand, for encapsulated MOSCAPs with \varnothing 240 μm , the variations corresponding to the four bending states on D_{it} at the energy level of $E_c-E = 0.37$ eV increased to 1.8, 3.4, 5.3, and 5.4 times. The variations on D_{it} at reference energy level in encapsulated MOSCAPs with \varnothing 320 μm importantly and stably increased to 1.1, 1.4, 1.4, and 1.4 times under four bending conditions. From the thorough analysis of D_{it} results, it can be carefully speculated that the interfacial characteristics of MOSCAPs with different gate dielectric surface areas under bending deformations are promoted/maintained overall through ultrathin encapsulation strategies of $\text{Al}_2\text{O}_3/\text{alucone}$ nanolaminates.

5. Conclusions

In conclusion, ultrathin encapsulation strategies of $\text{Al}_2\text{O}_3/\text{alucone}$ nanolaminates combined with different gate dielectric surface areas were employed in flexible monocrystalline Si NM based MOSCAPs and the electrical properties of encapsulated MOSCAPs with different gate dielectric islands were explored and evaluated under the planar and different bending deformations. The circular gate dielectric surface areas equipped with three types of \varnothing at 160 μm , 240 μm , and 320 μm performed different mechanisms under bending conditions. For encapsulated MOSCAPs with \varnothing of 160 μm , it can maintain the stability on C_{max} and frequency dispersion under concave and convex bending conditions, as well as have a certain ability to inhibit the growth of J_g compared to the bare MOSCAPs with the same \varnothing . As the \varnothing increased to \varnothing of 240 μm , it not only maintained the stability in C_{max} but strengthened the reliability in J_g and V_{fb} , while the performances on frequency dispersion accompanied with interfacial properties under convex bending deformations were supposed to be further optimized. The interfacial characteristics were enhanced under concave and convex bending conditions for encapsulated MOSCAPs at the largest \varnothing of 320 μm . However, the C_{max} deteriorated due to the high convex bending deformations the performances on J_g were decent in this configuration. These findings highlight that the different gate dielectric surface areas as form factors significantly influence the electrical performances in Si NM based MOSCAPs w/ and w/o encapsulation according to the concave and convex bending deformations. It is promising to use ultrathin encapsulation strategies to enhance the reliability and yields of high performance, long-lived flexible transistors based on ultrathin Si channel.

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Appendix

Material properties are fixed as follows: $E_{\text{Au}}=106$ Gpa [22], $\nu_{\text{Au}}=0.3$ [22], $E_{\text{Si}}=130$ Gpa [23], $\nu_{\text{Si}}=0.27$ [23], $E_{\text{Al}_2\text{O}_3}=163.3$ Gpa [24], $\nu_{\text{Al}_2\text{O}_3}=0.24$ [25], $E_{\text{HfO}_2}=73.4$ Gpa [24], $\nu_{\text{HfO}_2}=0.3$ [26], $E_{\text{alucone}}=44$ Gpa [27], $\nu_{\text{alucone}}=0.33$ [27].

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