APPENDICES

[Supplementary information]

Course and Tutorials

* 1. Online platform and Repositories

The DECEL project has a website and a Moodle section on which several resources have been deployed:

* DECEL website can be found at: [http://decel.eu](http://decel.eu/) it gives access to some resources listed in this document.
* Online course before the challenge (guest access): <https://celene.univ-tours.fr/course/view.php?id=15094>
* Online course during the challenge: <https://celene.univ-tours.fr/course/view.php?id=16438>
  1. Guided lab sheet

3 guided session allows the students to step up to finally run a B-mode ultrasound scan using the Red Pitaya-based ultrasound scanner.

1. Session 1: Ultrasound board and Redpitaya ecosystem (NB: acquire a first echo or RF line using the Redpitaya board as a simple scope) => <http://decel.univ-tours.fr/data/tutos/DECEL_week_tutorial1.pdf>
2. Session 2: Ultrasound imaging with Redpitaya (NB: trying to acquire a first image using Arduino board for the servo-motor control and the Redpitaya board with the default configuration and tools) => <http://decel.univ-tours.fr/data/tutos/DECEL_week_tutorial2.pdf>
3. Session 3: Dedicated low level solution (NB: guided implementation of modified HDL, middleware and software layers into Redpitaya board for the ultrasound imaging application) => <http://decel.univ-tours.fr/data/tutos/DECEL_week_tutorial3_v3.pdf>
   1. Register table of the FPGA-based modified HDL system on Redpitaya board

Supplementary information about the acquisition architecture (Fig. 1) and the register table (Table 1) implemented into the FPGA of the Red Pitaya board can be found bellow:

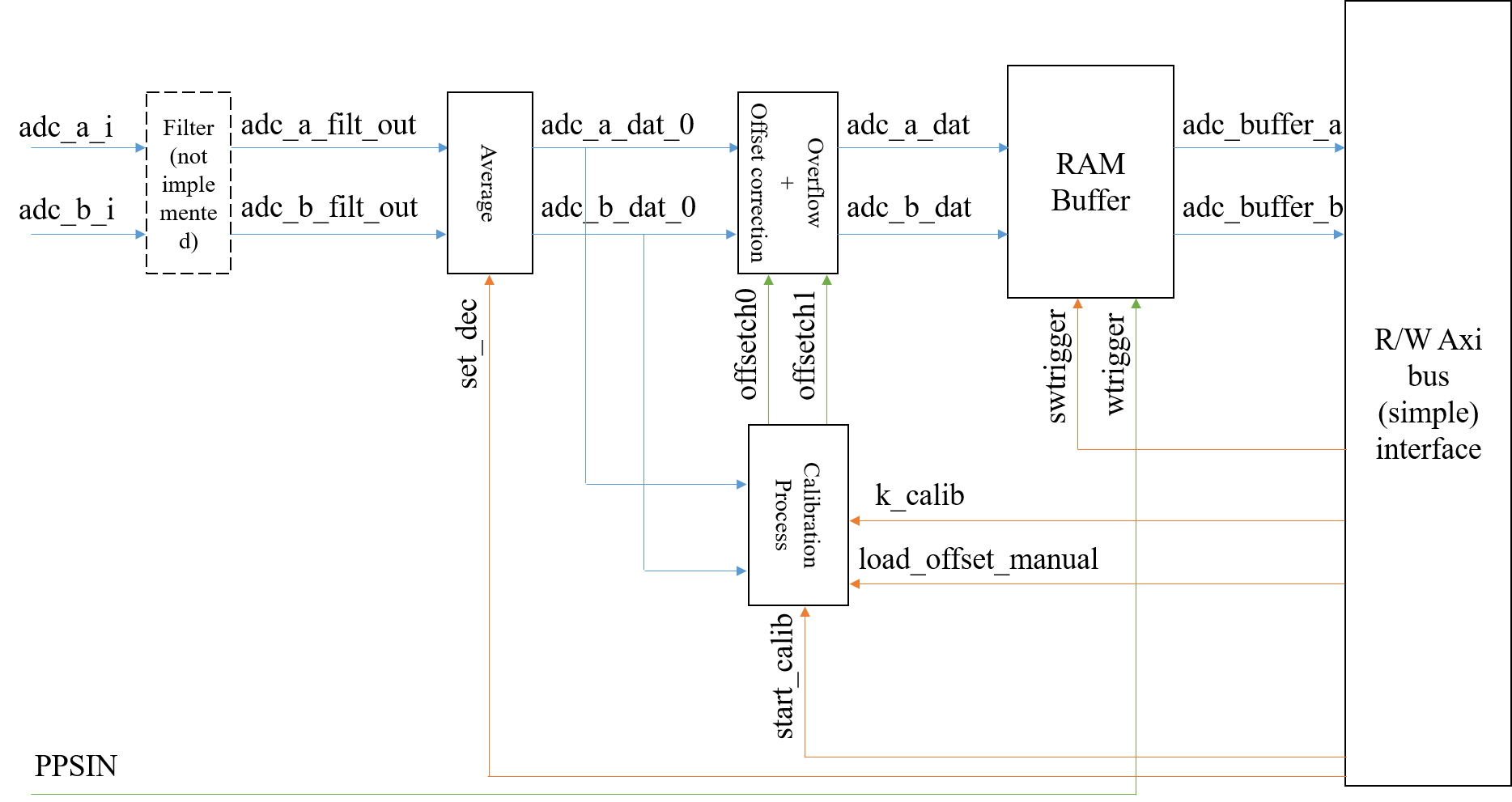


Figure 1 – Architecture of the default signal acquisition implemented on the FPGA.

**Table 1.** Register map implemented in the dedicated HDL implementation used by students:

Servo motor controller (output is pin DIO\_4N):

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Address** | **Function** | **Read, Write1** | **Bits2** | **Description** |
| 0x4010 0020 | Enable/disable servo controller | W/O | [0:0] | 1: enable generation of servo control signal  0: set servo control signal to zero |
| 0x4010 0024 | Servo trim | W/O | [7:0] | 8-bit signed offset added to the servo input data |
| 0x4010 0028 | Servo position | W/O | [9:0] | 10-bit signed position, zero is the middle position of the servo  -512 generates a 0.7 ms high pulse, +511 generates a 2.3 ms high pulse |

Output trigger generation (output trigger is pin DIO\_5N):

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Address** | **Function** | **Read, Write1** | **Bits2** | **Description** | |
| 0x4010 003C | Output trigger enable | W/O | [1:0] | | 0X: disable trigger generation, set output trigger to zero  10: enable software generated trigger (trigger is data written to 0x40100030)  11: enable hardware generated trigger |
| 0x4010 0030 | Software generated trigger | W/O | [0:0] | | If trigger enable is 102, the LSB of data written to this register is applied to the trigger output (pin DIO\_5N) |
| 0x4010 0034 | Hardware trigger period | W/O | [31:0] | | Period of the hardware trigger signal, in number of cycles of the 125 MHz clock. Default value is 12 500 000 for generating a 100 ms period (10 Hz) |
| 0x4010 0020 | Hardware trigger high-time | W/O | [31:0] | | Duration of the high-time of the trigger pulse, in number of cycles of the 125 MHz clock. Default value is 125 000 for a high-time equal to 1 ms |

Data acquisition:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Address** | **Function** | **Read, Write1** | **Bits2** | **Description** | |
| 0x4010 0014 | Decimation factor | RW | [15:0] | | Set the decimation factor to N, defaults to 16 (see note 3) |
| 0x4010 0018 | Decimation average mode | RW | [0:0] | | If set to 1, the output sample is the average of the previous N samples when N=1, 2, 4, 8 or 16, where N is the decimation factor; if set to 0 the output sample is the single sample acquired at each N samples (see note 3) |
| 0x4011 xxxx | Data RAM buffer channel A | R/O | [31:0] | | Reading from address 0x4011 0000 + (4\*addr), addr = 0..16383, reads the 32k 16-bit signed samples acquired from channel A (sample k in the low 16 bits, sample (k+1) in the high 16 bits). |
| 0x4012 xxxx | Data RAM buffer channel B | R/O | [31:0] | | Reading from address 0x4012 0000 + (4\*addr), addr = 0..16383, reads the 32k 16-bit signed samples acquired from channel B (sample k in the low 16 bits, sample (k+1) in the high 16 bits). See note 4. |
| 0x4010 0004 | Acquisition is idle | R/O | [0:0] | | Status of the acquisition process: 1=acquisition is idle waiting for trigger; 0= acquisition is running. |
| 0x4010 0010 | Arm signal acquisition | W/O | [0:0] | | Writing 1 to this register arms the signal acquisition process and the signal acquisition will start with the next trigger event, either a high pulse in pin DIO\_5P (input hardware trigger) or a software generated trigger (register 0x4010 0008) |
| 0x4010 0008 | Start signal acquisition | W/O | [0:0] | | Writing 1 to this register starts the signal acquisition process. This signal is OR’ed with the external hardware trigger input connected to pin the extension connector DIO\_5P. To start the acquisition, the process must be armed by writing 1 to register 0x4010 0010 (arm acquisition) |

Notes:

1 RW: read/write register, RO: Read only register, WO: Write only register

2 Only the bits referred are used by the logic circuit; signed data shorter than 32 bits is just truncated to the least N significant bits indicated.

3 The decimation factor sets the sampling frequency by dividing the master 125 MHz clock by the value loaded into this register (defaults to 16, Fs=7.8125 MHz). This can be any integer from 1 to 217-1=262143 (sampling frequencies from 125 MHz to 476.8 Hz) but if the averaging mode is active (register 0x40100018 – Average decimation - set to one) this value should be only set to the following values: 1: Fs=125 MHz, 2: Fs=62.5 MHz, 4: Fs=31.25 MHz, 8: Fs=15.625 MHz and 16: Fs=7.8125 MHz (defaults to 16, Fs=7.8125 MHz).

4 The data buffers should be accessed only when the acquisition process is not running, otherwise the signal retrieved may include samples from previous acquisitions. The acquisition process is inactive when reading 1 from register 0x4010 0004 (Acquisition is idle).

1. HDL and Software code repositories
   1. Students’ achievement and deliverables

International students participated in a course in Tours, where international teams

1. Students Deliverables

The students defended their project orally in front of several teachers. They demonstrated the results obtained with the hardware (Fig 2.) and presented a poster:

* Poster Team Amboise => <http://decel.univ-tours.fr/data/posters/Amboise.pdf>
* Poster Team Blois => <http://decel.univ-tours.fr/data/posters/Blois.pdf>
* Poster Team Chenonceau => <http://decel.univ-tours.fr/data/posters/Chenonceau.pdf>
* Poster Team Clos Lucé => <http://decel.univ-tours.fr/data/posters/Clos_Luce.pdf>
* Poster Team Villandry => <http://decel.univ-tours.fr/data/posters/Villandry.pdf>



Figure 2 - Some photo of the DECEL week. a) Oral assessment of the project. b) One of the team and his poster. c) All students and teachers attending. More outcomes (videos, etc.) can be found at decel.eu.

1. Students Feedback data

Raw data of the student feedback on the DECEL week in Tours can be found at => http://decel.univ-tours.fr/data/feedback/Student\_feedback\_on\_the\_DECEL\_week\_in \_Tours\_C2.csv.zip

1. Code repository

Even if all the code needed is already included in the tutorials, we list important code repositories here:

* Last version of the repository with several advanced features (to be used with Vivado 20.1): <http://decel.univ-tours.fr/data/DECEL_tuto3_V02.zip>
* Repository to be used in order to follow step by step the tutorial 3: <http://decel.univ-tours.fr/data/decel.zip>

Note: These repositories include code from HDL level, C code that can be built on Redpiatya embedded Linux and post-processing Matlab code. Please refer to [Tutorial 3](http://decel.univ-tours.fr/data/tutos/DECEL_week_tutorial3_v3.pdf) to use them correctly.