Preprints.org

Article

A Novel Lock-in Amplification-Based Frequency Component Extraction Method for Performance Analysis and Power Monitoring of Grid-Connected Systems

Abdur Rehman , Taeho An , Woojin Choi [*]

Article

A Novel Lock-in Amplification-Based Frequency Component Extraction Method for Performance Analysis and Power Monitoring of Grid-Connected Systems

Abdur Rehman, Taeho An and Woojin Choi *

School of Electrical Engineering, Soongsil University (06978), Seoul, Republic of Korea;
    engr.arehman98@gmail.com, anraeho@gmail.com

* Correspondence: cwj777@ssu.ac.kr

Abstract: In recent times, the increasing concern for climate control has led to the widespread application of grid-connected inverter (GIC) based renewable energy systems. In addition, the increased usage of non-linear loads and electrification of the transport sector cause ineffective grid-frequency management and the introduction of harmonics. These grid conditions affect power quality and result in uncertainty and inaccuracy in monitoring and measurement. Incorrect measurement leads to overbilling/underbilling, ineffective demand and supply forecasts for the power system, and inefficient performance analysis. To address the outlined problem, a novel three-phase frequency component extraction and power measurement method based on Digital Lock-in Amplifier (DLIA) and Digital Lock-in Amplifier Frequency-Locked Loop (DLIA-FLL) is proposed to provide accurate measurement under the conditions of harmonics and frequency offset. A combined filter with a lowpass filter and notch filter for DLIA is employed to improve computation speed. A comparative study is performed to validate the performance of the proposed power measurement method, by comparing the proposed method to the windowed interpolated fast Fourier transform (WIFFT). The ZERA COM 3003 (a commercial high-accuracy power measurement instrument) is used as the reference instrument in the experiment

1. Introduction

In the last decade, the increase in world population and extreme weather conditions has caused a rise in energy demand. The growth in energy demand results in increased production of electrical energy from fossil fuels, contributing to the deteriorating global warming crisis [1]. As a result, new policies related to decarbonization have been introduced by the global stakeholders to control and limit the worsening situation. The transition from conventional transportation means to electric vehicles (EVs) represents a significant step toward achieving the decarbonization goals for governments worldwide [1,2]. In addition, the penetration of grid-connected inverter (GCI) based renewable energy systems in the power system is increasing over time. Such increased integration results in reduced power system inertia that creates grid frequency management issues. The increased usage of grid-connected renewable energy systems, non-linear loads, and electrification of the transport sector results in non-sinusoidal grid conditions with harmonic injection and grid frequency deviations [3–7]. The non-sinusoidal grid conditions can result in the transformer overheating, tripping of power system equipment, and non-reliable power measurement by the conventional power measurement method used in watt-hour meters [6–8], and inefficient performance analysis of power electronics applications. For non-sinusoidal signals consisting of extra frequency components, component extraction is a critical part of achieving accurate power

measurement and performance analysis. Therefore, it is necessary to extract frequency components accurately [9–11].

Digital power measurement methods are becoming famous these days. This type of method records the samples of voltage and current and then calculates the instantaneous power in the time domain. It provides real-time measurement, stores big sizes of data, and is highly protected from tempering. Despite all the advantages of electronic power measurement methods, it is not suitable for measuring the power of a signal having harmonics and frequency fluctuations because of the error in zero-crossing detection which leads to inaccurate power measurement results [12–15]. In addition, it struggles to distinguish between different frequency components such as fundamental, harmonics, noise, and interharmonics. Ref [16] presents error analysis for digital input electricity meters, which utilize a time-domain approach for power measurement by taking the integration of input signal over time, which demonstrates a maximum power measurement error of 2% for a frequency offset of ± 0.5Hz shown in Figure 1.

(a)

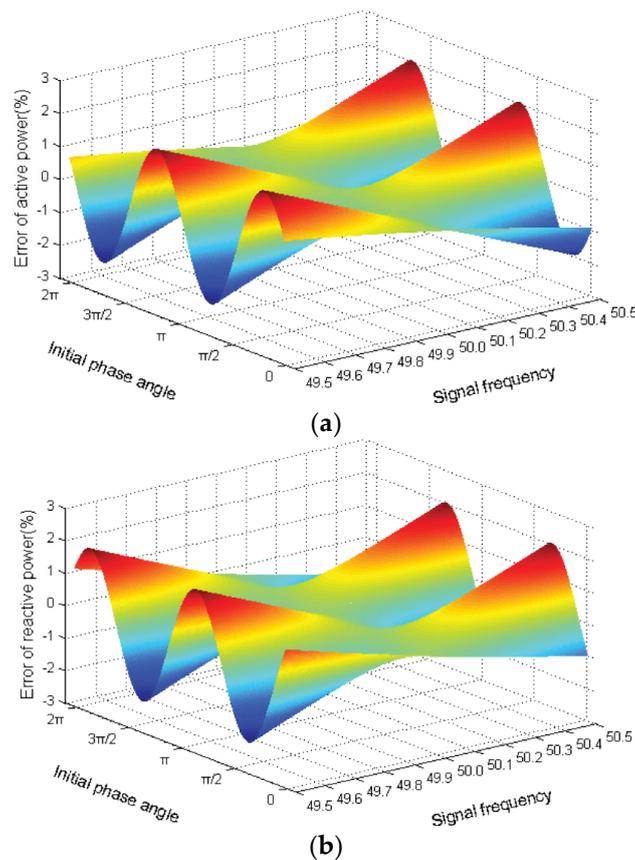(b)

Figure 1. Error curves for digital input electricity meters under the condition of ± 0.5Hz frequency offset (a) error in real power, (b) error in reactive power [16].

Fast Fourier transform (FFT) is another widely used method for the extraction of frequency components and using the extracted components for power calculation. The FFT method is very accurate when applied under the conditions of synchronous sampling [3,9]. However, the fundamental frequency deviation and introduction of harmonics make it difficult to maintain synchronous sampling in real-world applications. This results in inaccurate measurement due to the picket fencing and spectral leakage effects [17–19].

The literature introduced windowed FFT (WFFT) to reduce the effect of spectral leakage. In WFFT, different window functions are multiplied by the input signal followed by FFT calculation. The ideal window should have a low main lobe width and high roll-off for the side lobes to attain higher attenuation and better frequency resolution. There are different types of windows such as Hanning, Hamming, Blackman window, triangular self-convolution window, etc. Although the use

of WFFT improves the measurement results; the accuracy is still low as the ideal window cannot be selected because of the trade between the main lobe width and the side lobe attenuation [18,19].

Another solution proposed in the literature is the combined use of spectral correction technique and window function to reduce the effect of picket fencing and spectral leakage known as windowed interpolated FFT (WIFFT). In this method, the window function is applied to get the FFT result and then the spectral lines (double-spectrum-line or triple-spectrum-line) with maximum amplitude in the WFFT result are used to calculate the correction factors for the amplitude, frequency, and phase. WIFFT contains higher measurement accuracy as compared to the WFFT. However, WIFFT still has limitations if the frequency change is very fast, in that case, the result is inaccurate, and the use of window function with higher-order combined windows requires to solve the complex equations. As the power system is subject to frequency deviation and harmonic injection, these limitations cause non-reliable power measurements using FFT-based methods [19–21].

Digital Lock-in Amplifier (DLIA) is another method used to calculate power by extracting the voltage and current components for different frequencies. It has better performance in terms of component extraction as compared to the FFT [22–25]. In addition, the conventional DLIA has less computational burden as compared to FFT, as FFT works for a large range of evenly distributed frequency components and mostly requires complex window functions and interpolation. Table 1. shows the comparison of the computational burden of FFT and conventional DLIA for (N=10,000) [26]. However, DLIA has a limitation, under the condition of frequency deviation the measurement results become inaccurate [22–25].

Table 1. Comparison of computational burden of FFT and conventional LIA.

Operations	FFT [26]	Conventional DLIA [26]
Multiplications	>132878	1044

The literature demonstrates that many power measurement methods utilize feedback loops such as Frequency Locked Loop (FLL) and Phase Locked Loop (PLL) for tracking and synchronization purposes. The PLL methods include park transformation-based PLL and SOGI-PLL. The PLL-based method performs better around nominal grid frequency and for higher-order harmonics. However, the performance degrades for input signals with DC offset and low-order harmonics [27]. The FLL has more advantages as compared to PLL including the absence of a voltage control oscillator, which leads to reduced computational burden. However, it is observed that its performance deteriorates in the presence of disturbances such as DC offset and high total harmonic distortion (THD) [28]. A second-order generalized integrator-based FLL (SOGI-FLL) is introduced with an offset estimation and rejection loop [29]. However, it has the limitation that slightly wrong offset estimation results in measurement errors. Two more FLL-based methods, multiple adaptive vectorial filter-based FLL (MAVF-FLL) and reduced order generalized integrator-based FLL (ROGI-FLL), are proposed for frequency tracking. These methods are susceptible to DC offset and distorted input signals.

A prefilter-based frequency and phase estimation is proposed in ref [30], which relies on an additional frequency estimation technique to provide frequency information to be used by the prefilter. This additional loop resulted in increased complexity and computational burden. Similarly, ref [31] proposed a multi-circular limit cycle oscillator (multi-CLO-FLL). It also requires a prefilter to gain harmonic suppression ability. The currently available synchronization techniques face limitations and performance deterioration in an environment with disturbances such as DC offset and high THD. The solutions proposed to reject DC offset and suppress harmonics resulted in increased complexity and computational burden. Hence, there is a necessity to develop a power measurement method to overcome the limitations of conventional power measurement methods and give accurate results for the condition with frequency dynamics and harmonics.

This article proposes a novel frequency component extraction and three-phase power measurement method based on DLIAs and Digital Lock-in Amplifier Frequency-Locked Loop (DLIA-FLL) with combined filter to get accurate power measurement results for signals with

harmonics and frequency fluctuations. The DLIA-FLL tracks the fundamental frequency of the input signal followed by the generation of reference signals using tracked frequency. The DLIA uses the generated reference signals to extract the accurate amplitude and phase information for the fundamental and harmonic frequency components from the input voltage and current signals. These extracted parameters give accurate measurement results for electrical power parameters.

2. Proposed Frequency Component Extraction and Power Monitoring Method by Using DLIA and DLIA-FLL

The proposed component extraction method uses DLIA to extract the magnitude and phase information accurately for the fundamental and harmonic components present in the input signal. However, under the condition of frequency variation, the accuracy of DLIA decreases because of the difference between the frequency of reference signal and input signal. To cope with this limitation the proposed DLIA-FLL tracks any change in the frequency of input signal and updates the reference signals to be used by the DLIA for the component extraction. There are n number of DLIAs for voltage and current each, where n is the number of frequency components to be extracted. Figure 2. shows the block diagram of complete architecture of the proposed power measurement method with DLIA and DLIA-FLL.
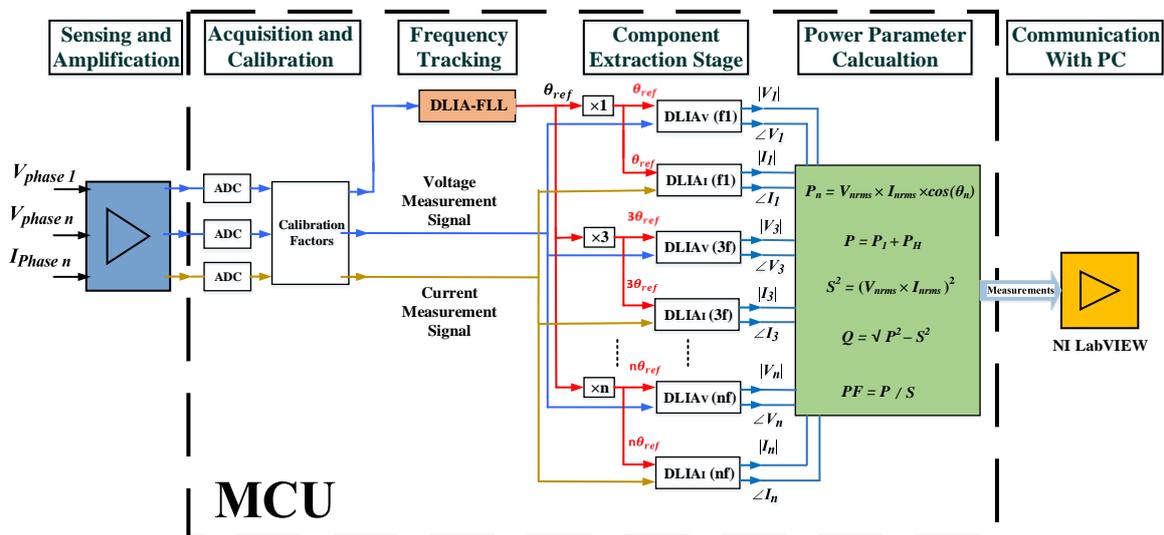

Figure 2. Block diagram of proposed the proposed component extraction and power measurement method with Digital Lock-in Amplifier Frequency Locked Loop (DLIA-FLL).

The voltage measurement signal that comes from the sensing and amplification stage, through ADC of the MCU, acts as the input for the proposed DLIA-FLL, which utilizes this input to track the fundamental frequency. In the next stage, these tracked frequency and measurement signals (voltage and current) that come from sensing and amplification stage, through ADCs of the MCU, act as the inputs for the DLIAs (DLIA1 - DLIAn), which utilize these inputs to extract the fundamental and harmonic frequency components. The extracted information of frequency components is represented in terms of magnitude and phase, which is further utilized to calculate the rms voltage, rms current, real power, reactive power, apparent power, phase difference, and power factor. In the final stage, the measurement results for voltage, current, frequency, and power are transferred to the PC (NI LabVIEW) through UART-Serial communication protocol.

Further explanation on the working principle of each component of the proposed power measurement method is given in sub-sections below.

2.1. Digital Lock-in Amplfier Working Principle

DLIA contains three sections, Phase Sensitive Detector (PSD), Combined Filter (CF), Phase and Amplitude extraction. Figure 3. shows the block diagram for DLIA.
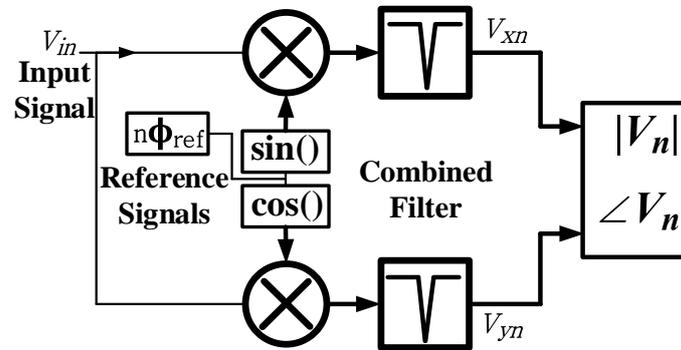

Figure 3. Block diagram for Digital Lock-in Amplifier (DLIA) with proposed combined filter (Lowpass Filter + Notch Filter).

In PSD the input signal is multiplied by the reference sine and cosine signals with a frequency the same as the frequency of the input signal to perform dual modulation Lock-in. Equation (1) shows the input voltage signal with fundamental and n odd harmonics.

$$V_{\text{sig}} = V_{amp} \begin{pmatrix} sin(\omega_f t + \theta_f) + \\ m_3 sin(3\omega_f t + 3\theta_f) + \\ \cdots \\ m_n sin(n\omega_f t + n\theta_f) \end{pmatrix}, \quad (1)$$

where V_{amp} is the peak amplitude of the fundamental component, m_n is the amplitude ratio of the nth harmonic with the amplitude of the fundamental component, ω_f is the frequency of the fundamental component, and θ_f is the phase information of the fundamental component (0,120,240 degrees) for the three-phase system.

Equation (2) shows the reference signals for DLIA. Where k defines the harmonic order of the reference signal, ω_{ref} is the frequency of the reference signal, and θ_{ref} is the phase information of the reference signal.

$$\begin{cases} V_{\sin\_ref} = sin\,(k\omega_{ref}t + k\theta_{ref}) \\ V_{\cos\_ref} = cos\,(k\omega_{ref}t + k\theta_{ref}) \end{cases}, \quad (2)$$

The dual-modulation Lock-in results in two signals, V_x and V_y by using the trigonometric identity. Equation (3) and (4) shows the simplified expression for V_x and V_y. These signals contain the amplitude of the concerned frequency component from the input signal at DC (0 Hz) and at twice the frequency of the concerned frequency component (120 Hz in this case) from the input signal.

$$V_x = \frac{V_{amp}}{2} \left[\sum_{\substack{n=1,3,\cdots \\ k=1,3,\cdots}} m_n \begin{Bmatrix} cos\left(\begin{matrix} (k\omega_{ref} - n\omega_f)t \\ +(k\theta_{ref} - n\theta_f) \end{matrix} \right) \\ -cos\left(\begin{matrix} (k\omega_{ref} + n\omega_f)t \\ +(k\theta_{ref} + n\theta_f) \end{matrix} \right) \end{Bmatrix} \right], \quad (3)$$

$$V_y = \frac{V_{amp}}{2} \left[\sum_{\substack{n=1,3,\cdots \\ k=1,3,\cdots}} m_n \begin{Bmatrix} sin\left(\begin{matrix} (k\omega_{ref} - n\omega_f)t \\ +(k\theta_{ref} - n\theta_f) \end{matrix} \right) \\ +sin\left(\begin{matrix} (k\omega_{ref} + n\omega_f)t \\ +(k\theta_{ref} + n\theta_f) \end{matrix} \right) \end{Bmatrix} \right], \quad (4)$$

The combination of single order low pass filter and the second-order notch filter is employed to extract the DC component from the V_x and V_y.

Equation (5) shows the transfer function for the combined filter. Where ω_c and k is the cut-off frequency and order of low pass filter respectively. ω_n is the natural frequency for notch filter. ζ_1 and ζ_2 are damping factor selected according to the condition ($\zeta_2 \ll \zeta_1$).

$$G_{CF}(s) = \left[\frac{s^2 + 2\zeta_2\,\omega_n\,s + \omega_n^2}{s^2 + 2\zeta_1\,\omega_n\,s + \omega_n^2}\right] \times \left[\frac{\omega_c}{s + \omega_c}\right]^k, \qquad (5)$$

The natural frequency of the notch filter is selected (120 Hz) as the lowest frequency component to be attenuated is twice the grid frequency. To attenuate the higher order frequency components single-order ($k = 1$) low pass filter with cut-off frequency ($\omega_c = 10$ Hz) is employed. Figure 4. shows the bode plot for the designed combined filter.
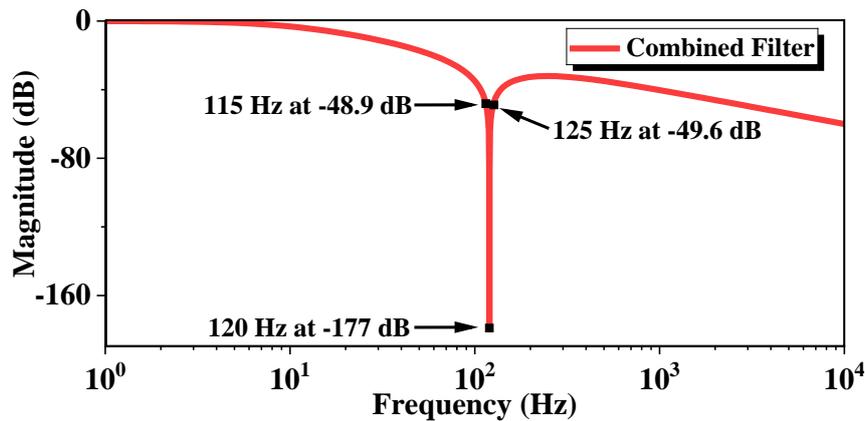

Figure 4. Bode plot for the combined filter consisting of notch filter and lowpass filter.

The application of the notch filter allowed the elimination of the lowest frequency component. As a result, a lowpass filter with reduced order and high cut-off frequency can be used. This proposed combined filter with low order and high cut-off leads to less computational burden and faster filter response [26]. It is important because computational burden is a critical factor in effective practical implementation of measurement method.

Equation (6) and (7) shows the signals at the output of the combined filters. These signals contain just DC component and 120 Hz. The other higher frequency components are attenuated.

$$V_d = \frac{V_{amp}}{2}\left[cos\left(\left(k\omega_{ref} - n\omega_f\right)t + \left(k\theta_{ref} - n\theta_f\right)\right)\right], \qquad (6)$$

$$V_q = \frac{V_{amp}}{2}\left[sin\left(\left(k\omega_{ref} - n\omega_f\right)t + \left(k\theta_{ref} - n\theta_f\right)\right)\right], \qquad (7)$$

In the last section of DLIA, the output signal of the combined filter section is used to calculate the amplitude and phase information of the desired frequency component. Equation (8) and (9) are used to calculate the amplitude and phase for the desired frequency component.

$$A_n = \sqrt{\left(\frac{V_{amp_n}}{2}\right)^2\left\{\begin{matrix}\left[cos\left(\left(k\omega_{ref} - n\omega_f\right)t + \left(k\theta_{ref} - n\theta_f\right)\right)\right]^2 \\ + \left[sin\left(\left(k\omega_{ref} - n\omega_f\right)t + \left(k\theta_{ref} - n\theta_f\right)\right)\right]^2\end{matrix}\right\}}, \quad (8)$$

$$\theta_n = \tan^{-1}\left\{\frac{\frac{V_{amp_n}}{2}\left[sin\left(\left(k\omega_{ref} - n\omega_f\right)t + \left(k\theta_{ref} - n\theta_f\right)\right)\right]}{\frac{V_{amp_n}}{2}\left[cos\left(\left(k\omega_{ref} - n\omega_f\right)t + \left(k\theta_{ref} - n\theta_f\right)\right)\right]}\right\}, \quad (9)$$

2.2. Digital Lock-in Amplfier Frequency-Locked Loop (DLIA-FLL)

The main objective of the proposed DLIA-FLL is to track the change in the grid-frequency to provide correct frequency f_{FLL} and phase θ_{FLL}. This frequency and phase information is used to

generate the correct reference signals for the DLIA to provide accurate extraction. Figure 5. shows the block diagram for the proposed DLIA-FLL.
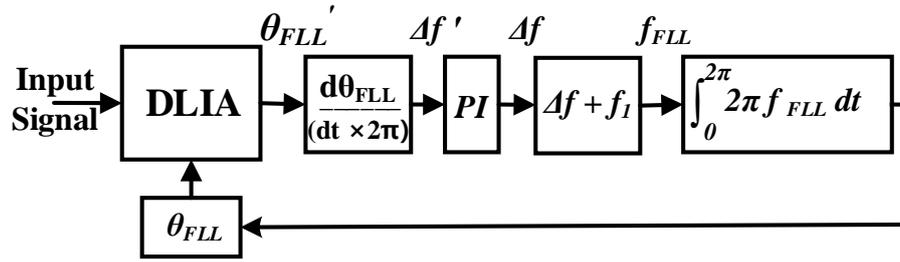

Figure 5. Block diagram for proposed reference signal synchronization method with Digital Lock-in Amplifier Frequency Locked Loop (DLIA-FLL).

The working principle of the DLIA-FLL is defined as the DLIA provides the phase output θ'_{FLL} using the output of the combined filter section shown in (10) that is further simplified to get (11).

$$\theta_{FLL}' = \tan^{-1}\left\{\frac{\frac{V_{amp_n}}{2}\left[sin\left((k\omega_{ref}-n\omega_f)t+(k\theta_{ref}-n\theta_f)\right)\right]}{\frac{V_{amp_n}}{2}\left[cos\left((k\omega_{ref}-n\omega_f)t+(k\theta_{ref}-n\theta_f)\right)\right]}\right\}, \quad (10)$$

$$\theta_{FLL}' = \left\{\left(k\omega_{ref}-n\omega_f\right)t+\left(k\theta_{ref}-n\theta_f\right)\right\}, \quad (11)$$

Equation (12) is used to find the difference in the frequency $\Delta f'$ by taking the derivative of phase θ'_{FLL} with respect to time.

$$\Delta f' = \frac{1}{2\pi} \times \frac{d}{dt}\left\{\left(k\omega_{ref}-n\omega_f\right)t+\left(k\theta_{ref}-n\theta_f\right)\right\}, \quad (12)$$

The resultant difference in frequency is passed through a PI controller which provides the updated difference in frequency Δf. This difference in frequency is added into the grid frequency (60 Hz in this case) to get tracked grid frequency f_{FLL} as shown in (13).

$$f_{FLL} = \Delta f + 60. \quad (13)$$

Equation (14) is used to calculate the phase of FLL which is then used to update the reference signals of DLIA.

$$\theta_{FLL} = \int_0^{2\pi} 2\pi f_{FLL}dt. \quad (14)$$

2.3. Component Extraction and Power Measurement by Proposed DLIA-FLL

As explained in the above sections, the DLIA-FLL tracks the grid-frequency and uses this information to update the reference signals for the DLIAs used in component extraction. The number of DLIAs are equal to the number of frequency components (DLIA1-DLIAn). These DLIAs extract the accurate amplitude and phase information for all the frequency components (fundamental and harmonics) input signals. The amplitude and phase for voltages and currents are used to calculate the real power, reactive power, apparent power, and power factor for each phase.

Equation (15) to (20) are used to estimate the power and power factor for non-sinusoidal conditions according to the standard formulas defined by IEEE Std 1459-2010 [32]. The power measurement results obtained by the proposed method are then transmitted from microcontroller unit (MCU) to the LabVIEW interface using UART communication to display the power measurement results.

$$P = P_1 + P_H, \quad (15)$$

$$P_1 = V_1 \times I_1 cos(\theta_1), \quad (16)$$

$$P_H = V_o \times I_o + \sum_{h\neq1} V_h \times I_h cos(\theta_h), \quad (17)$$

$$Q_1 = V_1 \times I_1 sin(\theta_1), \quad (18)$$

$$Q = \sqrt{P^2 - S^2}, \quad (19)$$

$$S^2 = (VI)^2, (20)$$

3. Experimental Implementation and Results

To validate the efficiency and accuracy of the proposed method, a three-phase power measurement experiment is carried out for 25% THD condition and an input signal with two different fundamental frequencies (60 Hz, and 61.5 Hz). The experimental results of the proposed method are compared with the results obtained from ZERA COM3003 and WIFFT (classical power measurement method). The below sections discuss the experimental setup and the results obtained from the power measurement experiment.

3.1. Experimental Setup and Configuration

The experimental setup and configuration used for the power measurement experiment is shown in Figure 6. The programmable AC source (Chroma 61704) is configured for the voltage (220 V per phase), current (4.48 A per phase), frequency (60 Hz, and 61.5 Hz), and harmonic profile for 25% THD.
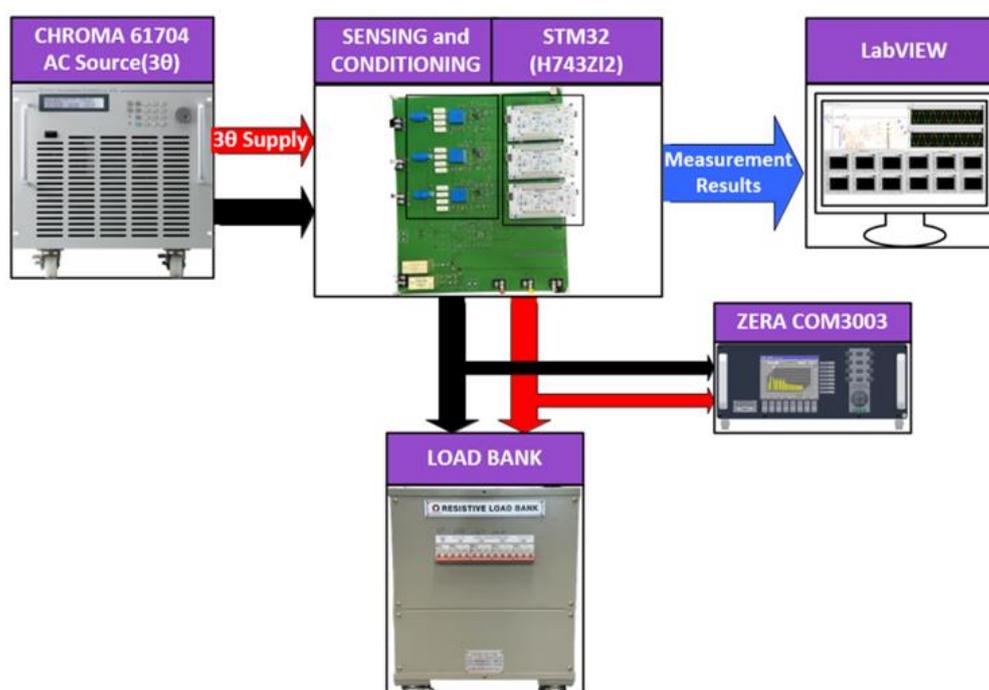

Figure 6. Experimental setup used for power measurement experiment.

After configuration, the output of the three-phase AC supply is connected to the input of the sensing and amplification circuit on the designed PCB. The developed sensor interface circuitry is based on LV 25-P for voltage sensing and LAH 50-P for current sensing. A 1.5V DC offset is added to the bi-polar measurement signals of voltage and current sensors to convert the signal into uni-polar form. The sensors are calibrated before the power measurement to remove the sensing and amplification stage error to the maximum. The temperature trends for sensors and sensor resistors are recorded, which leads to the selection of a consistent temperature (44 degrees Celsius for sensors and 40 degrees Celsius for sensing resistors) to avoid temperature-related drift in sensor performance during the experimentation.

The output of the sensing and amplification circuit is a unipolar voltage signal transmitted to the analog-to-digital converter (ADC) of the STM32 MCU. There are three MCUs based on the (H743ZIT6U) ARM Cortex-M7 digital signal processor. The MCU features an operating clock frequency of 480MHz, 16-bit ADC, 2MB of flash, and 1MB of RAM [33]. In addition, it offers a wide

range of peripherals including UART, SPI, I2C, and USB which makes it a suitable MCU for applications involving complex operations.

Each STM32 MCU has an algorithm based on the DLIA and DLIA-FLL for precise three-phase power measurement and frequency tracking. The input capture feature of the timer configuration in STM32 MCU is utilized to read external clock signal that helps to synchronize the interrupt generation and ADC acquisition of all the MCUs.

Figure 7. shows the flow chart for the algorithm inside STM32 MCU. At the start, there is an initialization of variables, ADCs, and interrupts. The MCU1 acts as a master and generates a pulse signal at general purpose input output pin (GPIO), which is read by other two slave MCUs to maintain the synchronized operation of all three MCUs. Following that the ADCs start the acquisition of voltage and current signals coming from the sensing and amplification circuit. The DLIA-FLL part of the algorithm uses the acquired signal amplitude to track the frequency of the input signal. Phase-1 voltage is used as the source of DLIA-FLL for all three phases. This process continues until 200 ms is completed. After that, the component extraction algorithm based on DLIA uses the acquired signals and tracked frequency from DLIA-FLL to extract the amplitude and phase for the fundamental and harmonic components.
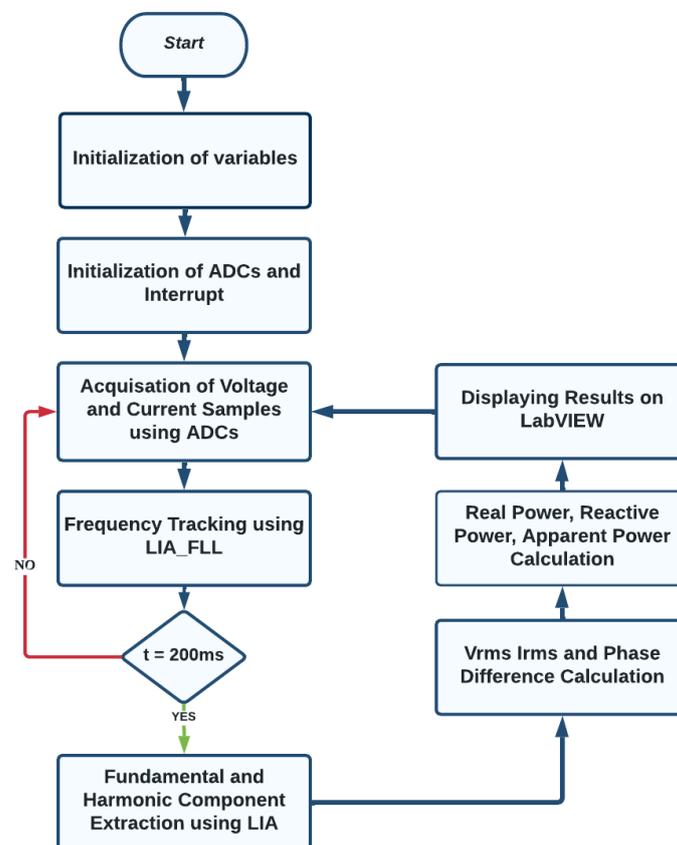

Figure 7. Flow chart for the proposed power measurement algorithm implemented in MCU.

The extracted information is used to calculate the rms voltage, rms current, and phase difference. This calculation leads to the calculation of real power, reactive power, apparent power, and power factor. All these power measurement results are then transferred to the LabVIEW interface with the help of UART communication. The LabVIEW interface displays the measurement result for each phase to validate and compare the performance.

The three-phase output of the PCB is connected to the load bank and ZERA COM3003. The ZERA COM3003, a commercial reference power measurement instrument is also connected in parallel to the load. Power measurement is also performed with ZERA COM3003 under the same testing conditions of voltage, current, frequency, and THD. The measurement results from ZERA

COM3003 are compared with the measurement results generated by the proposed method (DLIA and DLIA-FLL). The comparative analysis allows us to validate the accuracy and reliability of the proposed power measurement.

3.2. Frequency Tracking Results by the Proposed DLIA-FLL

The performance of the proposed DLIA-FLL is presented in this section. The experimental setup defined before is used with a sampling frequency of 40.02 kHz with 25% THD. This experiment is performed with two different cases of input signal frequency. In case a, the frequency of the input signal is fixed at 60 Hz and in case b the frequency of the input signal is changed to 61.5 Hz. The deviation in the frequency is selected according to the frequency deviation standard of ±1.5 Hz defined by the Korea Electric Power Company (KEPCO) [34]. The tracking results show that the developed DLIA-FLL algorithm inside the STM32 MCU tracks further frequency deviation in 151 ms. Figure 8. shows the frequency tracking results for frequency deviation from which it works well.
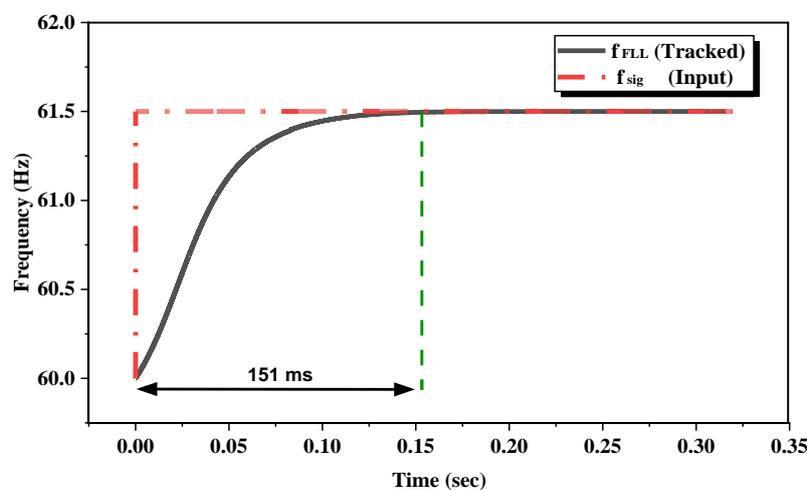

Figure 8. Frequency tracking results by proposed DLIA-FLL.

### 3.3. Component Extraction and Power Measurement by The Proposed DLIA-FLL and ZERA COM3003

This section explains the power measurement experiment performed with ZERA COM3003 and the proposed three-phase component extraction and power measurement method using the experimental setup explained before. After the definition of voltage, current, frequency, and THD profile with 25% THD, the Chroma AC power supply is used to provide the three-phase supply to the load through the designed PCB. The input signal frequency is set to 60 Hz. Figure 9. shows the three-phase voltage and current signals generated by chroma.

ZERA COM3003 is also connected to the system to perform the power measurement as well. Table 2. shows the THD measurement for three-phase system voltage using ZERA COM3003 respectively. It verifies that the generated THD is according to the defined THD profile.
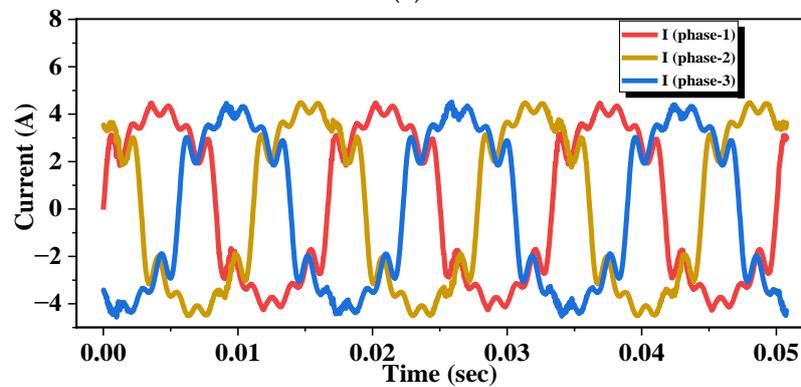
Table 2. Total harmonic distortion (THD) measurement results by ZERA COM3003 for three-phase voltage.

	Phase-1	Phas-2	Phase-3
V_1	100%	100%	100%
V_3	11.16%	11.14%	11.16%
V_5	11.16%	11.15%	11.15%
V_7	11.14%	11.12%	11.11%

V_9	11.00%	10.97%	10.99%
V_{11}	11.18%	11.16%	11.17%
THD_V	24.88%	24.85%	24.86%
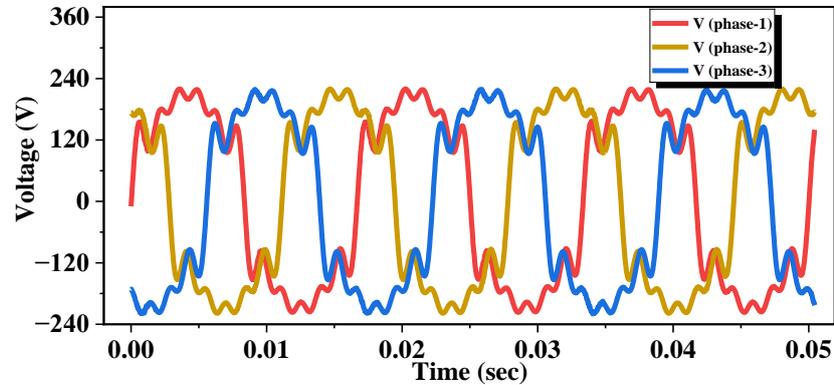
(a)

(b)

Figure 9. Three-phase voltage and current signals generated by chroma supply.

The proposed algorithm defined inside the STM32 MCU detects the voltage and current signals through the sensing and amplification circuit and performs the frequency tracking followed by component extraction and power calculation. The power measurement results are then sent to the LabVIEW interface through UART communication to display the results.

As explained earlier the ZERA COM3003 is connected to the experimental setup as the reference power measurement instrument. The comparative analysis is performed by calculating the percentage error by comparing the power measurement results obtained by the proposed DLIA-FLL to the power measurement results obtained by ZERA COM3003. The above-explained procedure is again repeated with the input signal frequency changed to 61.5 Hz under similar testing conditions of supply voltage, current, load, and THD.

Tables 3 and 4. show the comparative analysis results between the power measurement results obtained by the proposed DLIA-FLL and ZERA COM3003 for an input signal frequency of 60 Hz and 61.5 Hz respectively. The results show that the power measurement accuracy is ± 0.019% (accuracy class 0.02). The frequency tracking error under the frequency deviation is ± 0.005%.

Table 3. Measurement Results by the proposed DLIA-FLL for 60Hz fundamental signal.

	Phase-1	Phas-2	Phase-3
V_{rms} (V)	0.009%	0.010%	0.008%

	Phase-1	Phas-2	Phase-3
I_{rms} (A)	0.008%	0.009%	0.009%
P (W)	0.016%	0.016%	0.016%
Q (Var)	0.016%	0.017%	0.017%
S (VA)	0.017%	0.018%	0.017%
f (Hz)	0.004%	0.003%	0.004%

Table 4. Measurement Results by the proposed DLIA-FLL for 61.5 Hz fundamental signal.

	Phase-1	Phas-2	Phase-3
V_{rms} (V)	0.010%	0.008%	0.009%
I_{rms} (A)	0.008%	0.009%	0.009%
P (W)	0.018%	0.016%	0.018%
Q (Var)	0.017%	0.017%	0.018%
S (VA)	0.018%	0.017%	0.019%
f (Hz)	0.003%	0.004%	0.005%

3.4. Component Extraction and Power Measurement by WIFFT

Power measurement methods are generally based on different FFT methods. The WIFFT is a proposed method in recent literature to reduce the effect of picket-fencing and spectral leakage. The power measurement experiment is performed under the same testing conditions of voltage, current, load, and 25% THD. The input signal frequency is set to 60 Hz first and then changed to 61.5 Hz for the second measurement.

The WIFFT algorithm (with 1 Hz resolution) is defined in the MCU, which receives the voltage and current signals through a sensing and amplification circuit. WIFFT first calculates the WFFT and then uses the two spectral points with maximum amplitude to get the correction factors which are applied to get the amplitude, phase, and frequency of the voltage and current signal. These parameters lead to power calculation. The power measurement results are again sent to the same LabVIEW interface using UART communication to display the power measurement results. Tables 5 and 6. show the percentage error obtained by comparing the power measurement results obtained by WIFFT with the results obtained by ZERA COM3003. The results show that the power measurement error under the deviation is 0.051% and the frequency tracking error under the frequency deviation is ± 0.013%.

Table 5. Measurement Results by WIFFT for 60 Hz fundamental signal.

	Phase-1	Phas-2	Phase-3
V_{rms} (V)	0.011%	0.009%	0.008%
I_{rms} (A)	0.010%	0.010%	0.009%
P (W)	0.019%	0.019%	0.017%
Q (Var)	0.020%	0.018%	0.018%
S (VA)	0.017%	0.019%	0.017%
f (Hz)	0.005%	0.006%	0.005%

Table 6. Measurement Results by WIFFT for 61.5 Hz fundamental signal.

	Phase-1	Phas-2	Phase-3
V_{rms} (V)	0.022%	0.021%	0.019%
I_{rms} (A)	0.020%	0.029%	0.026%
P (W)	0.042%	0.051%	0.047%
Q (Var)	0.045%	0.053%	0.050%
S (VA)	0.043%	0.051%	0.047%
f (Hz)	0.012%	0.013%	0.011%

The comparison shows that for an input signal frequency of 60 Hz the proposed method has better performance as compared to WIFFT. However, under the condition of frequency deviation (61.5 Hz), the proposed method has much better performance (0.019%) as compared to WIFFT (0.051%). The reason for the deterioration in the performance of WIFFT is the fact that the 61.5 Hz causes the spectral leakage as the resolution is set to 1Hz with the (1 sec) data set, the resolution is non-integer multiple of input frequency, which results in incorrect results despite the window function and interpolation.

In case the frequency resolution observes variation the magnitude percentage error for WIFFT varies and follows the principle that if the resolution is an integer multiple of the input signal frequency, the resultant error is minimum and incase of non-integer multiple the error will be maximum. In between these two extreme conditions the magnitude of error will depend upon the degree of farness from integer multiple.

The results discussed above show that under the condition of frequency deviation and high THD, the proposed component extraction and three-phase power measurement method based on DLIA and DLIA-FLL has good performance under the frequency deviation ± 1.5 Hz and 25% THD. Though the proposed method is less accurate compared to the reference standard ZERA COM3003. However, this method is being developed for KEPCO to provide a cost-effective alternative compared to high-end power measurement devices with enough accuracy for applications such as inspection and performance analysis of devices such as wattmeter, inverters, and motor drives, for different conditions of frequency and THD focusing on power measurement and power quality.

4. Conclusions

In this article, a novel frequency component extraction method based on DLIA and DLIA-FLL, implemented inside the STM32 MCU, is proposed to get accurate component extraction and power measurement results under the conditions of harmonics and frequency fluctuations. The proposed DLIA-FLL tracks the frequency deviation of the input signal and provides the updated frequency which leads to the generation of reference signals for DLIA. The DLIA uses these updated reference signals to extract the amplitude and phase information from the input voltage and current signals. The introduction of a combined filter leads to a lower computational burden, which means less sampling frequency and faster computation. The extracted information leads to the calculation of real power, reactive power, apparent power, and power factor for each phase.

The validity and effectiveness of the proposed method are verified by conducting a power measurement experiment under the condition of 25% THD and two different input signal's fundamental frequencies (60 Hz and 61.5 Hz). The experimental setup consists of the PCB with sensing and amplification circuit and STM32 MCUs (containing proposed component extraction and measurement algorithm). The sensors are calibrated, and the temperature environment is kept consistent to mitigate any performance dynamics exhibited by sensing and conditioning circuit. The power measurement results are sent from MCUs to the LabVIEW interface through UART communication. The measurement results of the proposed method are compared with WIFFT and

the reference instrument ZERA COM3003. The comparison validates that the proposed method with DLIA and DLIA-FLL demonstrated better measurement accuracy compared to conventional methods such as WIFTT, for frequency variation of ± 1.5 Hz and under 25% THD condition.

References

1. Singh, A., Bhandari, S. & Kumar, J. Suppression of Harmonics in a Novel Multilevel Inverter Using Multi-Carrier Based PWM Technique. J. Electr. Eng. Technol. (2024). https://doi.org/10.1007/s42835-024-01907-7
2. F. Teng, Z. Ding, Z. Hu and P. Sarikprueck, "Technical Review on Advanced Approaches for Electric Vehicle Charging Demand Management, Part I: Applications in Electric Power Market and Renewable Energy Integration," IEEE Trans. Ind. Appl., vol. 56, no. 5, pp. 5684-5694, Sept.-Oct. 2020, doi: 10.1109/TIA.2020.2993991.
3. Zhang, H., Hu, X., Hu, Z. et al. Sustainable plug-in electric vehicle integration into power systems. Nat Rev Electr Eng 1, 35–52 (2024). https://doi.org/10.1038/s44287-023-00004-7
4. V. K. Tiwari, A. C. Umarikar and T. Jain, "Field Programmable Gate Array-Based Measurement System for Real-Time Estimation of Single-Phase Electric Power Quantities," IEEE Sensors J., vol. 19, no. 13, pp. 5086-5097, 1 July1, 2019, doi: 10.1109/JSEN.2019.2903855.
5. P. Vorobev, D. M. Greenwood, J. H. Bell, J. W. Bialek, P. C. Taylor and K. Turitsyn, "Deadbands, Droop, and Inertia Impact on Power System Frequency Distribution," IEEE Trans. Power. Syst., vol. 34, no. 4, pp. 3098-3108, July 2019, doi: 10.1109/TPWRS.2019.2895547.
6. Li, J., Yao, W., Wang, G. et al. A simple and fast measurement algorithm for power system flicker severity evaluation. Electr Eng (2024). https://doi.org/10.1007/s00202-024-02559-6.
7. A. Božiček, J. Kilter, T. Sarnet, I. Papič and B. Blažič, "Harmonic Emissions of Power Electronic Devices Under Different Transmission Network Operating Conditions," IEEE Trans. Ind. Appl., vol. 54, no. 5, pp. 5216-5226, Sept.-Oct. 2018, doi: 10.1109/TIA.2018.2808478.
8. S. Kannan, J. Meyer, J. Rens and P. Schegner, "A Novel Extended Noninvasive Harmonic Resonance Detection Technique for Public Low-Voltage Networks," IEEE Trans. Instrum. Meas., vol. 71, pp. 1-11, 2022, Art no. 9002711, doi: 10.1109/TIM.2022.3160548.
9. Babuta, A.; Gupta, B.; Kumar, A.; Ganguli, S. "Power and energy measurement devices: A review, comparison, discussion, and the future of research", Measurement, 2021, 172, 108961.
10. R. Morello, C. De Capua, G. Fulco and S. C. Mukhopadhyay, "A Smart Power Meter to Monitor Energy Flow in Smart Grids: The Role of Advanced Sensing and IoT in the Electric Grid of the Future," IEEE Sensors J., vol. 17, no. 23, pp. 7828-7837, 1 Dec.1, 2017, doi: 10.1109/JSEN.2017.2760014
11. H. Dirik, İ. U. Duran and C. Gezegin, "A Computation and Metering Method for Harmonic Emissions of Individual Consumers," IEEE Trans. Instrum. Meas., vol. 68, no. 2, pp. 412-420, Feb. 2019, doi: 10.1109/TIM.2018.2843538.
12. J. Paris, J. S. Donnal, Z. Remscrim, S. B. Leeb and S. R. Shaw, "The Sinefit Spectral Envelope Preprocessor," IEEE Sensors J., vol. 14, no. 12, pp. 4385-4394, Dec. 2014, doi: 10.1109/JSEN.2014.2334618.
13. M. K. Ikram, S. M. Amrr, M. S. J. Asghar, T. Islam and A. Iqbal, "Voltage Independent Reactive Current Based Sensor for Static VAr Control Applications," IEEE Sensors J., vol. 23, no. 9, pp. 10023-10031, 1 May1, 2023, doi: 10.1109/JSEN.2023.3258696. .
14. Z. Marais, H. E. van den Brom, G. Kok and M. G. A. van Veghel, "Reduction of Static Electricity Meter Errors by Broadband Compensation of Voltage and Current Channel Differences," IEEE Trans. Instrum. Meas., vol. 70, pp. 1-11, 2021, Art no. 1501511, doi: 10.1109/TIM.2020.3039631.
15. Q. Cetina, R. A. J. Roscoe and P. S. Wright, "Challenges for Smart Electricity Meters due to Dynamic Power Quality Conditions of the Grid: A Review," 2017 IEEE International Workshop on Applied Measurements for Power Systems (AMPS), Liverpool, UK, 2017, pp. 1-6, doi: 10.1109/AMPS.2017.8078345.
16. Z. Yan and H. Wen, "Performance Analysis of Electricity Theft Detection for the Smart Grid: An Overview," IEEE Trans. Instrum. Meas., vol. 71, pp. 1-28, 2022, Art no. 2502928, doi: 10.1109/TIM.2021.3127649.
17. W. Wu et al., "Effect of Frequency Offset on Power Measurement Error in Digital Input Electricity Meters," IEEE Trans. Instrum. Meas., vol. 67, no. 3, pp. 559-568, March 2018, doi: 10.1109/TIM.2017.2779538.

18. W. Li, G. Zhang, M. Chen, H. Zhong and Y. Geng, "Dynamic Harmonic Phasor Estimator Considering Frequency Deviation," IEEE Sensors J., vol. 21, no. 21, pp. 24453-24461, 1 Nov.1, 2021, doi: 10.1109/JSEN.2021.3113795.

19. A. Testa, D. Gallo and R. Langella, "On the Processing of harmonics and interharmonics: using Hanning window in standard framework," IEEE Trans. Power Del., vol. 19, no. 1, pp. 28-34, Jan. 2004, doi: 10.1109/TPWRD.2003.820437.

20. H. Qian, R. Zhao and T. Chen, "Interharmonics Analysis Based on Interpolating Windowed FFT Algorithm," IEEE Trans. Power Del., vol. 22, no. 2, pp. 1064-1069, April 2007, doi: 10.1109/TPWRD.2007.893187.

21. D. Belega, D. Dallet and D. Petri, "Accuracy of Sine Wave Frequency Estimation by Multipoint Interpolated DFT Approach," IEEE Trans. Instrum. Meas., vol. 59, no. 11, pp. 2808-2815, Nov. 2010, doi: 10.1109/TIM.2010.2060870.

22. H. Wen, J. Zhang, Z. Meng, S. Guo, F. Li and Y. Yang, "Harmonic Estimation Using Symmetrical Interpolation FFT Based on Triangular Self-Convolution Window," IEEE Trans. Ind. Informat., vol. 11, no. 1, pp. 16-26, Feb. 2015, doi: 10.1109/TII.2014.2362491.

23. J. A. F. Ferreira and A. Petraglia, "Analog integrated lock-in amplifier for optical sensors," IEEE Instrum. Meas. Magazine., vol. 20, no. 2, pp. 43-50, April 2017, doi: 10.1109/MIM.2017.7919134.

24. M. N. Ashraf, R. A. Khan and W. Choi, "A Novel Selective Harmonic Compensation Method for Single-Phase Grid-Connected Inverters," IEEE Trans. Ind. Electron., vol. 68, no. 6, pp. 4848-4858, June 2021, doi: 10.1109/TIE.2020.2989723.

25. B. K. Choudhury and P. Jena, "A Digital Lock-In Amplifier Assisted Active Islanding Detection Technique for DC Microgrids," IEEE Trans. Ind. Appl., vol. 59, no. 1, pp. 377-391, Jan.-Feb. 2023, doi: 10.1109/TIA.2022.3215165.

26. X. Fu, D. M. Colombo, H. H. Alamdari, Y. Yin and K. El-Sankary, "Lock-In Amplifier for Sensor Application Using Second Order Harmonic Frequency With Automatic Background Phase Calibration," IEEE Sensors J., vol. 22, no. 16, pp. 16067-16080, 15 Aug.15, 2022, doi: 10.1109/JSEN.2022.3191128.

27. S. Jana and S. Srinivas, "A Computationally Efficient Harmonic Extraction Algorithm for Grid Applications," IEEE Trans Power. Del, vol. 37, no. 1, pp. 146-154, Feb. 2022, doi: 10.1109/TPWRD.2021.3054554.

28. M. Xie, H. Wen, C. Zhu and Y. Yang: DC Offset Rejection Improvement in Single-Phase SOGI-PLL Algorithms: Methods Review and Experimental Evaluation. IEEE Access, vol. 5, pp. 12810-12819, 2017, doi: 10.1109/ACCESS.2017.2719721.

29. S. Golestan, J. M. Guerrero, F. Musavi and J. C. Vasquez, "Single-phase frequency-locked loops: A comprehensive review", IEEE Trans. Power Electron., vol. 34, no. 12, pp. 11791-11812, Dec. 2019.

30. S. Vazquez, J. A. Sanchez, M. R. Reyes, J. I. Leon, and J. M. Carrasco, ''Adaptive vectorial filter for grid synchronization of power converters under unbalanced and/or distorted grid conditions,'' IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1355–1367, Mar. 2014.

31. A. Sahoo, J. Ravishankar and C. Jones, "Phase-locked loop independent second-order generalized integrator for single-phase grid synchronization", IEEE Trans. Instrum. Meas., vol. 70, pp. 1-9, 2021.

32. H. Ahmed, M. Bierhoff and M. Benbouzid, "Multiple nonlinear harmonic oscillator-based frequency estimation for distorted grid voltage", IEEE Trans. Instrum. Meas., vol. 69, no. 6, pp. 2817-2825, Jun. 2020.

33. IEEE Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal, Nonsinusoidal, Balanced, or Unbalanced Conditions, IEEE Std 1459-2010 (Revision of IEEE Std 1459-2000), vol., no., pp.1-50, 19 March 2010, doi: 10.1109/IEEESTD.2010.5439063.

34. ST Microelectronics. (2020, march). Getting started with the STM32H7 Series MCU 16-bit ADC. Available at: https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf

35. CyberKEPCO. Available online: https://cyber.kepco.co.kr/ckepco/front/jsp/CO/H/htmlView/COHAHP00908.jsp#