A Unified Semiconductor-Device-Physics-Based Ballistic Model for the Threshold Voltage of Modern Multiple-gate MOSFETS

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Article

A Unified Semiconductor-Device-Physics-Based Ballistic Model for the Threshold Voltage of Modern Multiple-gate MOSFETS

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Abstract: Based on the minimum conduction band edge caused by the minimum channel potential resulting from the quasi-3D scaling theory and the 3D density of state (DOS) accompanied by the Fermi-Dirac distribution function on the source and drain sides, a unified semiconductor-device-physics-based ballistic model is developed for the threshold voltage of modern multiple-gate (MG) transistors, including FinFET, W-gate MOSFET, and Nanosheet (NS) MOSFET. It is shown that the thin silicon, thin gate oxide, and high work function will alleviate the ballistic effects and resist the threshold voltage degradation. Besides, as the device dimension is further reduced to give rise to the 2D/1D DOS, the lowest conduction band edge is hence increased to resist the threshold voltage degradation. The nanosheet MOSFET exhibits the largest threshold voltage among the three transistors due to the smallest minimum conduction band edge caused by the quasi-3D minimum channel potential. Compared to P-type MOSFET (P-FET), the N-FET shows more threshold voltage because the electron has a more effective mass than the hole.

Keywords: Quasi-3D scaling theory; W-gate MOSFET; FinFET; nanosheet transistor; ballistic effects; ballistic threshold voltage; Fermi-Dirac distribution function; density of state (DOS); effective mass

1. Introduction

The modern multiple-gate (MG) MOSFET is superior to planar MOSFET in suppressing the short-channel effects (SCEs) and supporting a higher driving current and packing density. Among the MG transistors, the proposed triple-gate (TG) MOSFET (i.e., FinFET)[1][2][3] with the ultra-thin silicon body and 3D gate oxide coverage can enhance the switching speed and decrease more electrostatic power consumption than the double-gate (DG) MOSFET proposed as the first non-planar MOSFET with the unique volume conduction [4][5]. Meanwhile, to further increase the IC packing density to accommodate the future GPU for trillion transistor counts, the 3D IC has converted the conventional lateral CMOS layout into the vertical gate-stacked CFET [6][7][8]. The nanosheet MOSFET [9][10][11] comprising CFET has been recognized as an alternative to FinFET and served as the basic building block for the implementation of the next-generation 3D ULSI. As the device feature size is further reduced toward 3nm/2nm, semiconductor node, the free carriers can directly arrive in the drain side without backscattering due to the feature size being smaller than the mean free path. This implies that the traditional drift-diffusion model (DDM), based on the thermal equilibrium between the free carriers and the lattice, is no longer accurate for developing the model of device behavior. Instead of DDM, the ballistic transport model (BTM) should be applied to model the device. The threshold voltage is one of the essential semiconductor device parameters that must be carefully monitored when the 3D ULSI is evaluated for its electrostatic power consumption to achieve power saving. In this work, a unified threshold voltage model for the ballistic FinFET, ◎-gate MOSFET, and nanosheet transistor is achieved based on the quasi-3D scaling theory, the density of state (DOS), and the Fermia-Dirac distribution function. It is shown that the thin silicon, thin gate oxide, and high work function will alleviate the ballistic effects and resist the threshold voltage degradation. Besides, the nanosheet MOSFET exhibits the largest threshold voltage among the three

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transistors due to the smallest minimum conduction band edge. As the device height/width is further reduced to bring about 2D/1D DOS for the MG MOSFETs, the threshold voltage will be increased to some extent because the 2D/1D DOS can induce a smaller carrier concentration than the 3D DOS for the transistors.

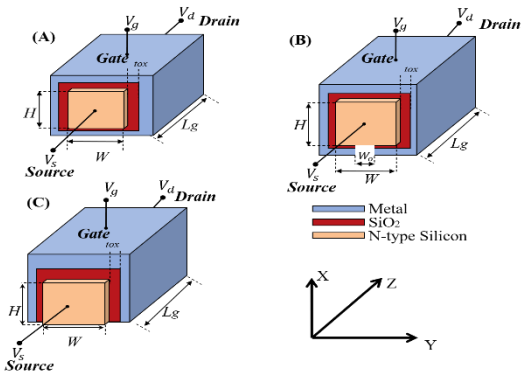

Figure 1. Typical schematic of the 3D modern multiple-gate MOSFETs composed of (A) nanosheet (NS) MOSFET, (B) W-gate MOSFET, and (C) FinFET. The channel direction is along with the z-axis. The channel length, height, and width are denoted by L_g, H, and W, respectively. The gate oxide thickness is denoted by t_{ox}.

2. Model Description

(A) Quasi-3D scaling theory for the ballistic MG MOSFETs:

As the device is further scaled down to work in the subthreshold regime, where the electrical field parallel to the channel direction strongly affects the device's behavior, the channel potential of F_{MC} can be governed by the quasi-3D scaling theory by accounting for the short-channel effects [12]:

$$\frac{d^2\Phi_{MC}(z)}{dz^2}+\frac{\Phi_{MC}(z)-\phi_{MCL}}{\lambda_{MG}^{\ 2}}=0 \quad (1)$$

with

$$\begin{cases}\phi_{MCL}=V_{gs}-V_{fb}-\dfrac{qN_a\lambda_{MG}^{\ 2}}{\varepsilon_{si}}\\ \dfrac{1}{\lambda_{MG}^{\ 2}}=\dfrac{1}{\theta^2}\left(\dfrac{\rho}{\lambda_{SG-x-z}^{\ 2}}+\dfrac{1-\rho}{\lambda_{DG-x-z}^{\ 2}}+\dfrac{1}{\lambda_{DG-y-z}^{\ 2}}\right)\end{cases} \quad (2)$$

$$\begin{cases}\lambda_{SG-x-z}=\sqrt{\dfrac{(2C_H+C_{ox})H^2}{2C_{ox}}},\lambda_{DG-x-z}=\sqrt{\dfrac{(4C_H+C_{ox})H^2}{8C_{ox}}}\\ \lambda_{DG-y-z}=\sqrt{\dfrac{(4C_W+C_{ox})W^2}{8C_{ox}}},\alpha=\dfrac{W_o}{W}\end{cases} \quad (3)$$

$$C_H=\frac{\varepsilon_{si}}{H},C_W=\frac{\varepsilon_{si}}{W},C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}},V_{fb}=\Phi_m-\Phi_s \quad (4)$$

where f_{MCL} is the long-channel bulk potential. The 3D scaling length l_{MG} in (1) can be expressed in (2), where l_{SG-x-z}, l_{DG-x-z}, and l_{DG-y-z} are the 2D scaling lengths for the single-gate and double-gate MOSFETs residing in the x-z and y-z cut-plane, respectively. θ $(1\le\theta<2)$ considers the coupling effects between the x-z and y-z planes and a is the ratio of single-gate oxide to the entire gate oxide in the y-z cut plane. For nanosheet MOSFET, one obtains ρ =0; for FinFET MOSFET, we have ρ =1. However, 0< ρ <1 should be used to develop the 3D scaling length for W-gate MOSFET, W_o is the opening at the bottom gate oxide of W-gate FET. The channel width, height, and gate oxide thickness

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in (3) are denoted by W, H, and t_{ox}. The difference in work function between the gate material and silicon body causes the flat-band voltage of V_{fb} in (4). The solution of (1) can be obtained as

$$\Phi_{MC}(z) = Te^{\frac{-\lambda_{MG}}{z}} + Ue^{\frac{\lambda_{MG}}{z}} + \phi_{MCL} \quad (5)$$

With the boundary conditions of $F_{MC}(z=0)=V_{bi}$, $F_{MC}(Z=L_g)=V_{bi}+V_{ds}$, the coefficients for T and U in (5) can be obtained as

$$T = \frac{(V_{bi} - \phi_{MCL})e^{L_g/\lambda_{MG}} - (V_{bi} + V_{ds} - \phi_{MCL})}{2\sinh(L_g/\lambda_{MG})} \quad (6)$$

$$U = -\frac{(V_{bi} - \phi_{MCL})e^{-L_g/\lambda_{MG}} - (V_{bi} + V_{ds} - \phi_{MCL})}{2\sinh(L_g/\lambda_{MG})} \quad (7)$$

where V_{ds} and V_{bi} are the drain voltage and built-in potential at the junction between the source/drain and channel. With (6) and (7), the minimum channel potential for the ballistic MG MOSFETs can be expressed as

$$\Phi_{\min} = 2\sqrt{TU} + V_{gs} - V_{fb} - \frac{qN_a\lambda_{MG}^2}{\varepsilon_{si}} \quad (8)$$

Both T and U in (8) can be linearized for V_{gs}, which leads to

$$T = \alpha V_{gs} + \beta \ , \ U = \kappa V_{gs} + \delta \quad (9)$$

with

$$\alpha = \frac{1 - e^{L_g/\lambda_{MG}}}{2\sinh(L_g/\lambda_{MG})}, \ \beta = \frac{(V_{bi} + V_{fb} + \frac{qN_a\lambda_{MG}^2}{\varepsilon_i})(e^{\frac{L_g}{\lambda_{MG}}} - 1) - V_{ds}}{2\sinh(L_g/\lambda_{MG})} \quad (10)$$

$$\kappa = \frac{e^{-L_g/\lambda_{MG}} - 1}{2\sinh(L_g/\lambda_{MG})}, \ \delta = \frac{V_{ds} - (V_{bi} + V_{fb} + \frac{qN_A\lambda_{MG}^2}{\varepsilon_{si}})(e^{\frac{-L_g}{\lambda_{MG}}} - 1)}{2Sinh(L_g/\lambda_{MG})} \quad (11)$$

(B) Free electron concentration for the ballistic MG MOSFETs:

The free electron concentration for the MG MOSFETs by considering the ballistic transport mode (BTM) can be expressed as:

$$n = \int_{E_{C,\min}}^{\infty} g_v \times D(E) \times [f_s(E) - f_d(E)]dE \quad (12)$$

where g_v is the silicon degeneracy, D(E) is the density of state (DOS), which has been divided by 2 by considering the electron per spin in calculating free electron concentration, $f_s(E)$ and $f_d(E)$ are the Fermin-Dirac distribution function on the source/drain sides, respectively. The 3D DOS in (12), by considering the 3D wave equation, can be obtained as

$$D(E) = \frac{4\pi m^* \sqrt{2m^*(E - E_{C,\min})}}{h^3} \quad (13)$$

with

$$E_{C,\min} = E_C - q\Phi_{\min} \quad (14)$$

where m^* is the effective mass of the electron and $E_{C,min}$ is the minimum conduction edge caused by the minimum channel potential of F_{min} shown in (8). The Fermi-Dirac distribution function on the source/drain sides can be expressed as

$$f_s(E) = \frac{1}{1 + e^{(E - F_{FS})/kT}}, \ f_d(E) = \frac{1}{1 + e^{(E - F_{Fd})/kT}} \quad (15)$$

with

$$E_{Fd} = E_{Fs} - qV_{ds} \quad (16)$$

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where E_{Fd} and E_{Fs} are the quasi-Fermi levels on the drain/source sides, respectively. By substituting (13), (14), (15), and (16) into (12), the free electron concentration for the ballistic MG MOSFETs can be obtained as

$$n = \frac{g_v T_o \left(\sqrt{2kTm^* \pi}\right)^3}{h^3} \left[F_{1/2}(\eta_{Fs}) - F_{1/2}(\eta_{Fd})\right] \quad (17)$$

with

$$\begin{cases} F_{1/2}(\eta_{Fs}) = \dfrac{2}{\sqrt{\pi}} \int_0^{+\infty} \eta^{1/2} \left(\dfrac{1}{1+e^{\eta-\eta_{Fs}}}\right) d\eta \\ F_{1/2}(\eta_{Fd}) = \dfrac{2}{\sqrt{\pi}} \int_0^{+\infty} \eta^{1/2} \left(\dfrac{1}{1+e^{\eta-\eta_{Fd}}}\right) d\eta \end{cases} \quad (18)$$

and

$$\begin{cases} \eta_{Fs} = \dfrac{(E_{Fs} - E_{C,\min})}{kT}, \ \eta_{Fd} = \dfrac{(E_{Fs} - qV_{ds} - E_{C,\min})}{kT} \\ E_{Fs} = E_C - \left(\dfrac{E_G}{2} + kT \ln \dfrac{N_d N_a}{n_i^2}\right) \end{cases} \quad (19)$$

where $F_{1/2}(\eta_{Fs})$ and $F_{1/2}(\eta_{Fs})$ are the fermi-Dirac integral of order 1/2. For the non-degenerate carrier statistics (i.e., Maxwell Boltzmann statistics), (17) can be further reduced as

$$n = \frac{g_v \left(\sqrt{2kTm^* \pi}\right)^3}{h^3} e^{\frac{E_{Fs}-E_C}{kT}} e^{\frac{\Phi_{\min}}{V_T}} \left(1 - e^{\frac{-qV_{ds}}{kT}}\right) \quad (20)$$

because the Fermi-Dirac integral of any order can be reduced as exponential terms (i.e., $F_i(h)=e^h$), which is shown as follows:

$$\begin{cases} F_{1/2}(\eta_{Fs}) = \dfrac{2}{\sqrt{\pi}} \int_0^{+\infty} \eta^{1/2} \left(\dfrac{1}{1+e^{\eta-\eta_{Fs}}}\right) d\eta \approx e^{\eta_{Fs}} \\ F_{1/2}(\eta_{Fd}) = \dfrac{2}{\sqrt{\pi}} \int_0^{+\infty} \eta^{1/2} \left(\dfrac{1}{1+e^{\eta-\eta_{Fd}}}\right) d\eta \approx e^{\eta_{Fd}} \end{cases} \quad (21)$$

(C) Criterion of threshold voltage for the ballistic MG MOSFETs:

To attain the threshold condition, the minority carrier concentration of n-FET should be equal to the majority carrier concentration of p-FET. This implies that the electron concentration of n in N-FET should be equal to N_a of P-substrate by assuming the complete impurity ionization (i.e., $p \approx N_a$) in P-FET. According to the criterion of threshold condition, the threshold voltage of gate bias should satisfy the following criterion:

$$n\big|_{V_{gs}=V_{th}} = N_a \quad (22)$$

where V_{th} is the threshold voltage. By substituting (22) into (20), the minimum channel potential corresponding to the threshold criterion can be obtained as

$$\Phi_{\min,3D} = V_T \ln \left(\frac{N_a h^3}{g_v \left(\sqrt{2kTm^* \pi}\right)^3 e^{\frac{E_{Fs}-E_C}{kT}} \left(1 - e^{\frac{-qV_{ds}}{kT}}\right)} \right) \quad (23)$$

From (8), (9), (10), (11), and (23), the threshold voltage can be achieved by solving for the quadratic equation of V_{gs}. This leads to

$$V_{th} = \frac{S - \sqrt{S^2 - 4RV}}{2R} \quad (24)$$

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with

$$\begin{cases} R=(1-4\alpha\kappa)\ ,\ S=2\gamma+4(\beta\kappa+\alpha\delta) \\ V=\gamma^2-4\beta\delta,\ \gamma=\Phi_{\min,3D}+V_{fb}+\dfrac{qN_a{\lambda_{MG}}^2}{\varepsilon_{si}} \end{cases} \quad (25)$$

It should be noted that the BTM brings about the new minimum channel potential shown in (23), which can uniquely determine the threshold voltage for the ballistic MG MOSFETs.

(D) Free electron concentration for the low-dimensional ballistic MG MOSFETs:

As the device height/weight is shrunk and compatible/smaller than the electron wavelength (~2nm), the 2D/1D DOS should be applied to derive the free electron concentration for the device. The 2D/1D DOS for the MG transistors can be obtained by solving the 2D/1D wave equation. This leads to

$$\begin{cases} D_{2D}(E)=\left(\dfrac{2\pi m^*}{h^2}\right) \\ D_{1D}(E)=\sqrt{\dfrac{m^*}{2h^2\left(E-E_{C,\min}\right)}} \end{cases} \quad (26)$$

$D_{2D}(E)$ and $D_{1D}(E)$ have considered the spin per electron. According to the similar developing procedure as shown in (12), the 2D/1D free electron concentration can be expressed as

$$n_{2D}=\left(\frac{2m^*g_vkT}{h^2}\right)\left[F_0(\eta_{Fs})-F_0(\eta_{Fd})\right] \quad (27)$$

$$n_{1D}=\left(\sqrt{\frac{m^*\pi}{2}}\frac{g_v}{h}\right)\left[F_{-1/2}(\eta_{Fs})-F_{-1/2}(\eta_{Fd})\right] \quad (28)$$

where $F_0(h_F)$ and $F_{-1//2}(h_F)$ are the Fermi-Dirac integral of order 0 and -1/2, respectively. They can be expressed as

$$\begin{cases} F_0(\eta_F)=\int_0^{+\infty}\dfrac{1}{1+e^{\eta-\eta_F}}d\eta \\ F_{-1/2}(\eta_F)=\dfrac{1}{\sqrt{\pi}}\int_0^{\infty}\dfrac{\eta^{-1/2}}{1+e^{\eta-\eta_F}}d\eta \end{cases} \quad (29)$$

Similarly, in terms of non-degenerate carrier statistics, (27) and (28) can be further reduced as

$$n_{2D}=\left(\frac{2m^*g_vkT}{h^2}\right)e^{\frac{E_{F1}-E_C}{kT}}e^{\frac{\Phi_{\min}}{V_T}}\left(1-e^{\frac{-qV_{ds}}{kT}}\right) \quad (30)$$

$$n_{1D}=\left(\sqrt{\frac{m^*\pi}{2}}\frac{g_v}{h}\right)e^{\frac{E_{F1}-E_C}{kT}}e^{\frac{\Phi_{\min}}{V_T}}\left(1-e^{\frac{-qV_{ds}}{kT}}\right) \quad (31)$$

(E) Criterion of threshold voltage for the low-dimensional ballistic MG MOSFETs:

By setting free electron density equal to the substrate doping concentration, as shown in (22), the criterion of threshold voltage for 2D and 1D MG devices can be shown as

$$\Phi_{\min,2D}=V_T\ln\left(\frac{N_a\times W\times h^2}{\left(2\pi g_vm^*kT\right)e^{\frac{E_{F1}-E_C}{kT}}\left(1-e^{\frac{-qV_{ds}}{kT}}\right)}\right) \quad (32)$$

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$$\Phi_{\min,1D} = V_T \ln\left(\frac{N_a \times W \times H \times h}{g_v\left(\sqrt{0.5 \times m^* kT\pi}\right)e^{\frac{E_{F1}-E_C}{kT}}\left(1-e^{\frac{-qV_{ds}}{kT}}\right)}\right) \quad (33)$$

By replacing $F_{min,3D}$ with $F_{min,2D,}$ and $F_{min,1D}$, the threshold voltage for 2D and 1D MG MOSFETs can be obtained.

3. Results and Discussion

The 3D device simulator "SDEVICE" is employed to validate the proposed model [14]. Unless otherwise stated, the following device parameters are used to simulate the MG MOSFETs: the device structure's square shape, the effective electron mass =1.08m_0, and the valley degeneracy of the silicon g_v=6. The graded density model is included to simulate the carrier density. Also, the quantum-potential model simulates the electrostatic potential, ensuring that the Poisson equation is self-consistent with the wave equation. Figure 2 plots the threshold voltage versus the channel length of FinFET for different silicon thicknesses. As the channel length decreases, the thin silicon can produce a larger threshold voltage than the thick silicon due to the alleviated ballistic effects that result in threshold voltage degradation. Figure 3 plots the threshold voltage versus the channel length of W-gate MOSFET for different oxide thicknesses. The thin gate oxide that effectively resists the ballistic effects can induce a smaller threshold voltage degradation than the thick gate oxide. Figure 4 shows how the work function affects the threshold voltage as the channel length is decreased for nanosheet MOSFET. The high work function can bring about a high threshold voltage as the channel length decreases, as opposed to the low work function, which reduces the threshold voltage due to the strong ballistic effects. To show how the different dimensionalities of the devices affect the threshold voltage. Figure 5 uses the different ratio of device width to device height (i.e., W × H) by considering (2nm × 2nm), (2nm × 5nm), and (5nm×5nm) cross-section area of FinFET with the channel length decreased from 20nm to 10nm. Note that as the device dimension is approaching the electron wavelength (~2nm), the 2D/1D density of state should be accounted for in calculating the electron concentration, as shown in Figure 5. It is shown that the 1D device with the cross-section area of 2nm × 2nm can induce the largest threshold voltage as opposed to the 3D device with the cross-section area of 5nm × 5nm, which results in the smallest threshold voltage because the high-dimensional device cannot effectively alleviate the ballistic effects that degrade the threshold voltage. Figure 6 shows the threshold voltage versus the channel length for different devices' structures, including nanosheet MOSFET. W-gate MOSFET, and FinFET. The nanosheet MOSFET exhibits the largest threshold voltage and smallest threshold voltage degradation with the gate surrounding the channel regime. However, FinFET, with the smallest gate coverage, will show the smallest threshold voltage and largest threshold voltage degradation among the three devices. It is known that the scaling factor can provide the designing guidance for the threshold voltage of the MG devices. Figure 7 plots the threshold voltage versus the scaling factor for different silicon and oxide combinations of the FinFET. It can be seen that as the scaling factor is reduced below 3, the threshold voltage will be significantly degraded. Therefore, when designing the MG MOSFETs, the allowable silicon/oxide thickness combinations corresponding to the appropriate scaling factor should be carefully accounted for.

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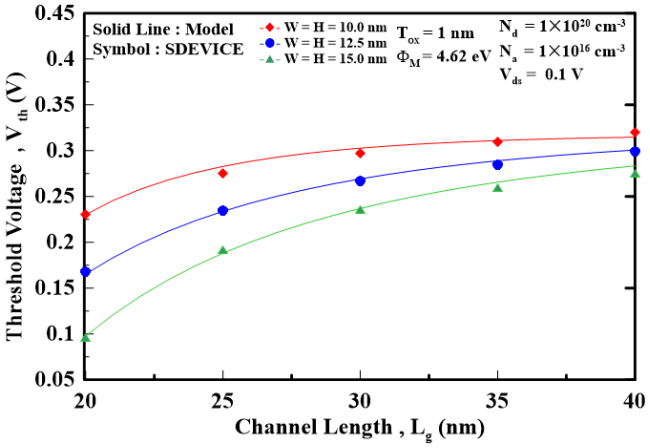

Figure 2. threshold voltage versus the channel length for different silicon thicknesses of the FinFET.

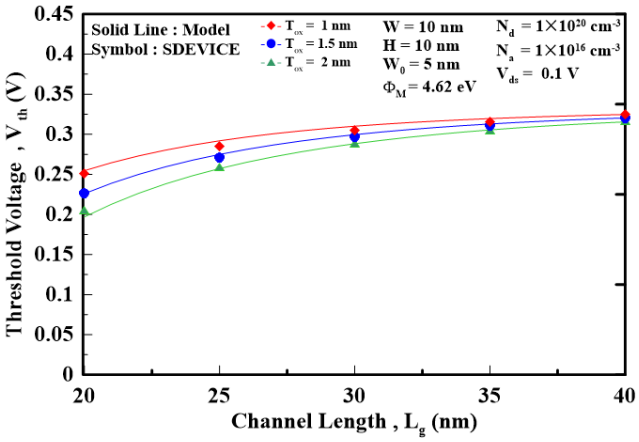

Figure 3. threshold voltage versus the channel length for different gate oxide thicknesses of the W-gate MOSFET.

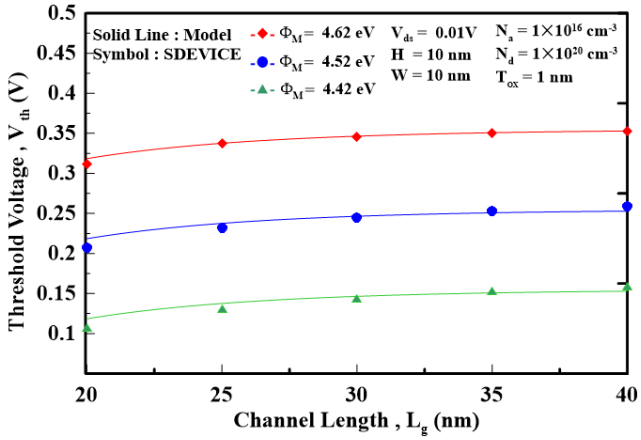

Figure 4. threshold voltage versus the channel length for different work functions of the nanosheet MOSFET.

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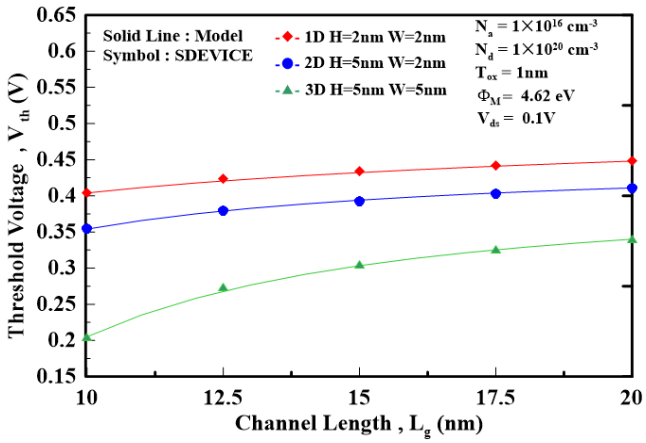

Figure 5. threshold voltage versus the channel length for different dimensionalities of the FinFET.

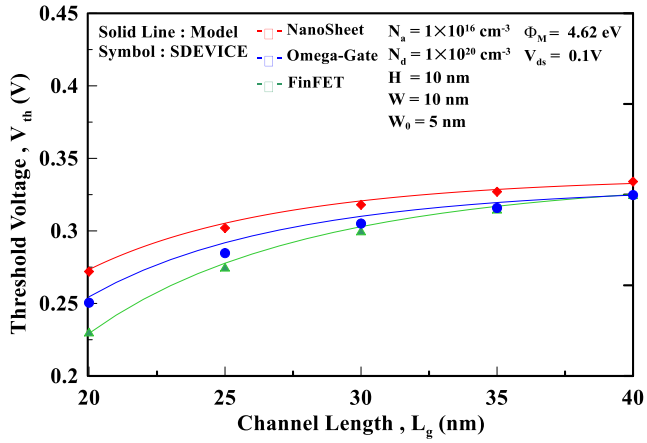

Figure 6. threshold voltage versus the channel length for different MG FETs, including FinFET, W-gate MOSFET, and nanosheet MOSFET.

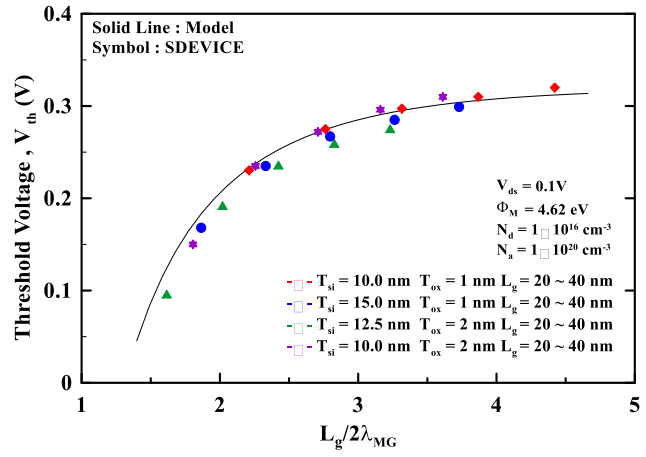

Figure 7. threshold voltage versus the scaling factor for silicon/oxide thickness combinations of the FinFET.

4. Conclusion

As for the modern multiple-gate (MG) transistors composed of FinFET, W-gate MOSFET, and nanosheet MOSFET, a unified ballistic model for the threshold voltage is proposed and validated.

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The model can also be applied for P-type MG devices by interchanging the device parameters between electron and hole. Accompanied by P-type MG MOSFET, the modern complementary gate-stacked MOSFET (i.e., CFET) can be integrated to simulate the subthreshold logic circuit for its low-power circuit application.

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