Communication

A 0.8V Low-Power Wide-Tuning Range CMOS VCO for 802.11ac and IoT C-Band Applications

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A 0.8V Low-Power Wide-Tuning Range CMOS VCO for 802.11ac and IoT C-Band Applications

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Abstract: This paper presents a 0.8 V low-power CMOS voltage-controlled oscillator (VCO) with a wide tuning range, fabricated using a TSMC 0.18-μm process. The proposed design incorporates body-biasing techniques and an optimized varactor structure to achieve a tuning range of 1124 MHz (5.829–4.705 GHz) and low phase noise of −117.6 dBc/Hz at a 1 MHz offset. Operating at an ultra-low supply voltage of 0.8 V, the VCO consumes only 3.4 mW, demonstrating excellent power efficiency. A buffer circuit is also employed to enhance output symmetry and suppress flicker noise without introducing additional control complexity. With a figure-of-merit (FOM) of −188.6 dBc/Hz and a wide tuning range of 22.2%, the proposed VCO is well-suited for modern low-power communication systems, including 802.11ac, 5G transceivers, satellite links, and compact IoT devices.

Keywords: VCO; tuning range; phase noise; low-power design; C-band; body-bias technique; CMOS RF circuits; IoT applications

1. Introduction

In modern wireless and optical communication systems, efficient voltage-controlled oscillators (VCOs) play a critical role in signal generation. CMOS VCOs have been widely utilized due to their cost-effectiveness and compatibility with System-on-Chip (SoC) integration. However, achieving a wide tuning range and low power consumption while maintaining low phase noise remains a challenge in traditional designs.

Previous research has extensively investigated the fundamental limitations of phase noise and power efficiency in CMOS VCO designs [1–4]. Several techniques have been proposed to optimize phase noise performance, including approaches aimed at minimizing flicker noise and enhancing the tuning range [4–7]. More recent studies have introduced advanced techniques such as switched-biasing and resistive tuning to achieve low-power operation and wide frequency tunability. However, these techniques generally suffer from increased design complexity, limited reduction in power consumption, or constrained frequency tuning ranges. Therefore, designing a VCO that simultaneously achieves ultra-low power consumption, low phase noise, wide tuning range, and simplified circuit architecture remains a significant challenge and warrants further exploration.

This work presents a novel CMOS VCO that employs body-bias technology and an optimized buffer circuit to significantly extend the tuning range and enhance power efficiency. Operating at an ultra-low voltage of 0.8 V, the proposed design demonstrates substantially reduced power consumption compared to conventional designs typically requiring supply voltages of 1.2 V or higher. The design achieves a wide tuning range of 1124 MHz and maintains excellent phase noise performance, making it an attractive solution for 5G, satellite communications, and optical networking applications.

2. VCO Design

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2.1. Phase Noise

In addition to the noise generated by the circuits, noise from the power supply also affects phase noise [8–10]. Using the transistor as the tail current source can decrease the noise from the power supply to the VCO. For PMOS-only VCO, the active region provides the VCO better protection against noise from the power supply [11].

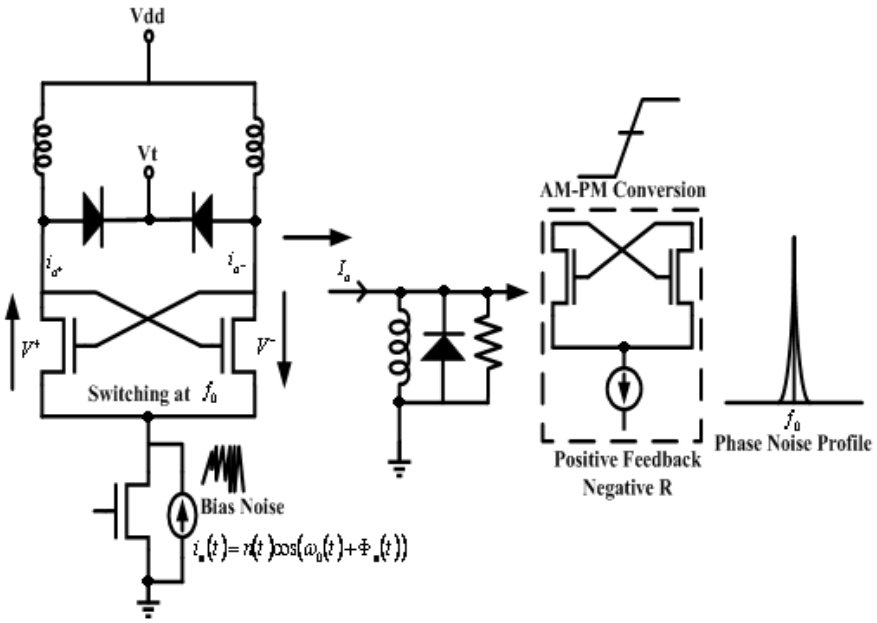

Figure 1. Conversion of bias noise into phase noise.

That the phase noise improves as quality factor Q increases. The Q of standard inductor L1 is around 8.62, and the Q value of the center tapped inductor L3 is around 5.39. The LC-tank Q is about 7.9, and the impedance at resonance frequency is about 0.75 Ω which is shown in Figure 2.

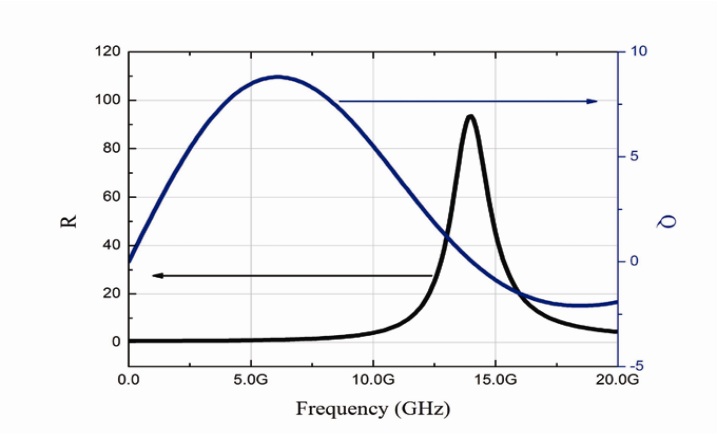

Figure 2. Simulated impedance and quality factor versus frequency characteristics in the LC tank.

2.2. VCO Design

The cross-coupled pair is used to suppress parasitic effects introduced by the transistors. It can increase the ratio of tuning capacitance (C_v) and parasitic capacitance ($C_{parasitic}$). High C_v/ $C_{parasitic}$ ratio can achieve a wider frequency tuning range. The PMOS varactor C_v value at different control voltage is shown in Figure 3. Figure 3 shows a good C_{max}/C_{min} ratio of about 2.78 which can be achieved in a

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0.18um bulk CMOS technology with a tuning voltage ± 2V. The oscillator frequency can be determined with Equation (1).

$$f_{OSC} = \left(2\pi\sqrt{L\left(C_{ind} + C_v + C_{MOS}\right)}\right)^{-1} \quad (1)$$

where C_{ind} is the equivalent parallel capacitance of the inductor, C_v is the equivalent capacitance of one varactor, and C_{MOS} is the equivalent parallel capacitance of the NMOS crossed-coupled transistor.

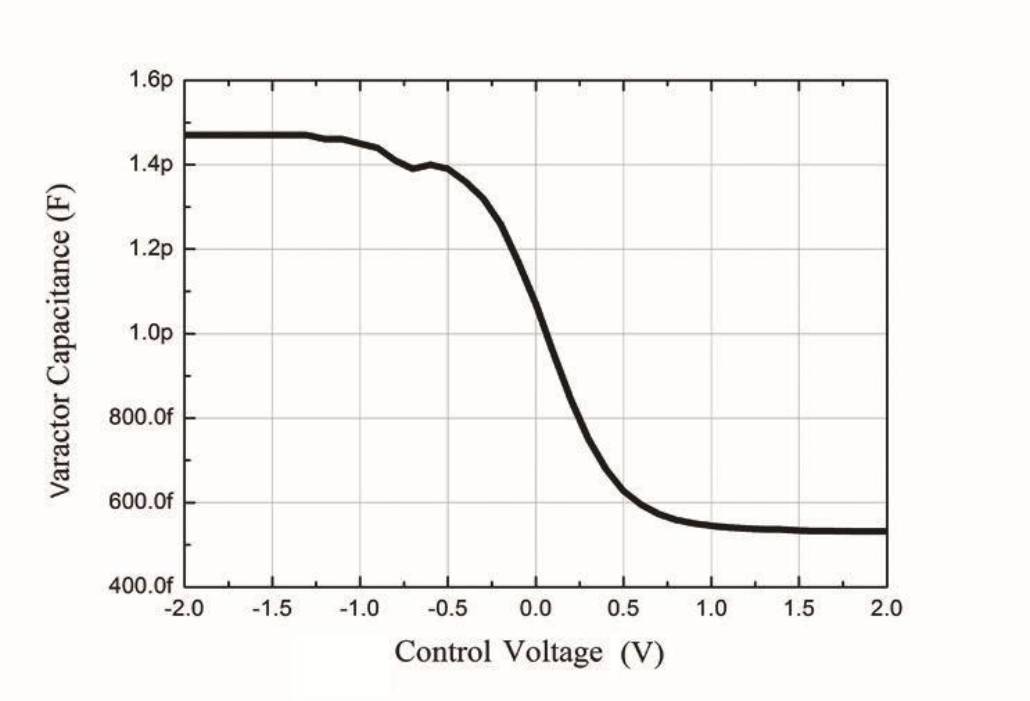

Figure 3. Simulation C-V curve of the PMOS varactor.

The architecture of the proposed VCO is based on a negative resistance LC-tank oscillator with an NMOS cross-coupled pair (M_1 and M_2) as the core active components, is shown in Figure 4. The tuning mechanism utilizes a pair of varactors (C_1, C_2), controlled by the tuning voltage (V_t), enabling frequency adjustment between 5.829 GHz and 4.705 GHz.

To achieve low power consumption, the circuit operates at a reduced supply voltage of 0.8V. A body-biasing technique is applied to transistors M_3 and M_4, lowering the threshold voltage and enabling operation with minimal power dissipation. This results in a measured power consumption of 3.4 mW. For phase noise optimization, a buffer stage comprising transistors M_5, M_6, and inductors L_3, L_4 is included to enhance the output signal swing and minimize phase noise degradation.

Although switched-biasing techniques effectively reduce flicker noise, they typically require additional control circuits, which increase design complexity and power consumption. Instead, our approach utilizes a carefully designed buffer circuit to achieve a comparable improvement in phase noise while maintaining ultra-low power consumption. The measured phase noise at 1 MHz offset is -117.6 dBc/Hz. The buffer circuit also improves waveform symmetry, reducing flicker noise contributions and enhancing overall signal integrity.

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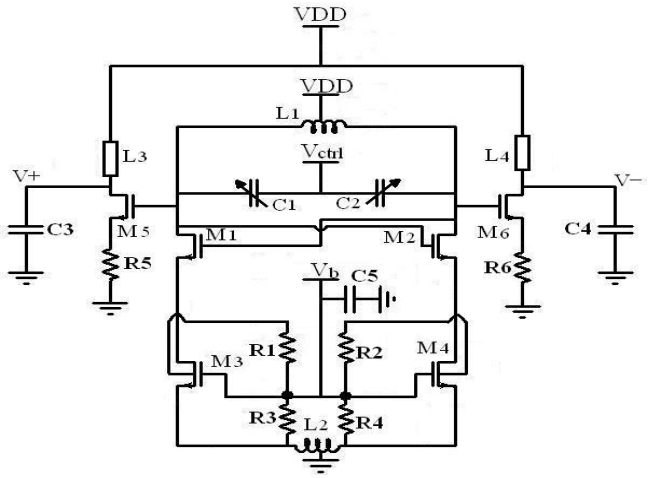

Figure 4. Circuit schematic of the VCO.

3. Simulation and Measurement Results

3.1. Simulation Results

In Figure 5, the simulated phase noise of the VCO is -116.5dBc/Hz. The tuning range is from 5.8 GHz to 4.5 GHz with control voltage varied from 0 to 1.2 V, as shown in Figure 6.

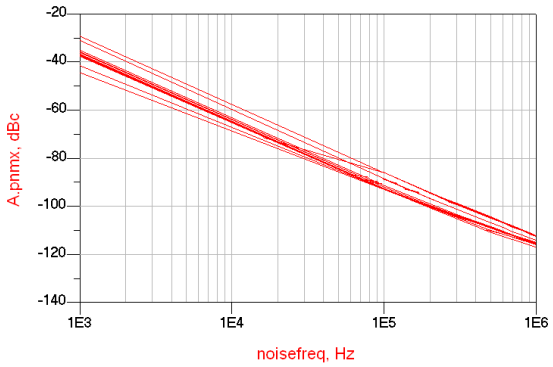

Figure 5. Simulation result of the phase noise.

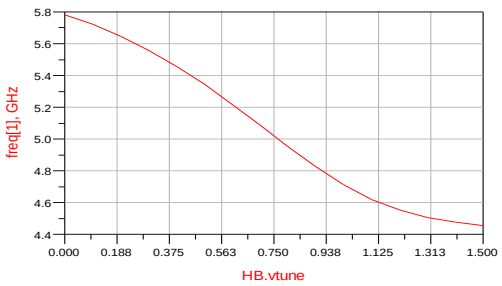

Figure 6. Simulated tuning range of the VCO.

3.2. Measurement Results

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The VCO circuit is designed and fabricated in TSMC's 0.18-μm CMOS process. The process offers six metal layers for interconnect, and various kinds of RF inductors and varactors. The physical dimensions of the low-phase-noise VCO chip is 0.499 mm² including pads. The VCO die photo is shown in Figure 7. The measured tuning range is 1124 MHz for control voltage from 0~1.3 V. The VCO exhibits a wide tuning range of 22.2%, as shown in Figure 8. Figure 9 shows the phase noise measurement results. The phase noise at the offset frequencies of 1 MHz is -117.69 dBc/Hz. The frequency spectrum of VCO at 5.06 GHz with power of -22.44 dBm is shown in Figure 10. The FOM value is about -196.6 dBc/Hz and it is calculated using the FOM defined as [12]:

$$FOM = L\{f_{offset}\} - 20 \cdot \log\left(\frac{f_0}{f_{offset}}\right) + 10 \cdot \log\left(\frac{P_{DC}}{1mW}\right) \quad (2)$$

f_0 is the oscillation frequency, $L\{f_{offset}\}$ is the measured phase noise at offset frequency f_{offset}, and P_{DC} is the DC power consumption in mW. The power-frequency-tuning-normalized (PFTN) factor of the proposed VCO is calculated as [13]:

$$PFTN = 10 \cdot \log\left[\left(\frac{TR}{f_{offset}}\right)^2 \cdot \frac{kT}{P_{DC}}\right] - L\{f_{offset}\} \quad (3)$$

TR is the tuning range and k is Boltzmann's constant. A temperature of $300^o K$ is used for the PFTN calculation.

Table 1 compares the VCO post-simulation and our measured results. Table 2 compares the performance of VCOs based on different CMOS technologies from five previous studies. Most studies use CMOS technology with 0.18 μm, except for [16], which uses 0.13 μm. All designs operate around 5 GHz, with a frequency range of 5.0 to 5.3 GHz. Although our result has slightly worse phase noise performance (-117.7 dBc/Hz) than other studies, it achieves the widest tuning range (22.2%) and the lowest power consumption (3.4 mW) while maintaining a competitive FOM. These characteristics are ideal for low-power wireless communication applications.

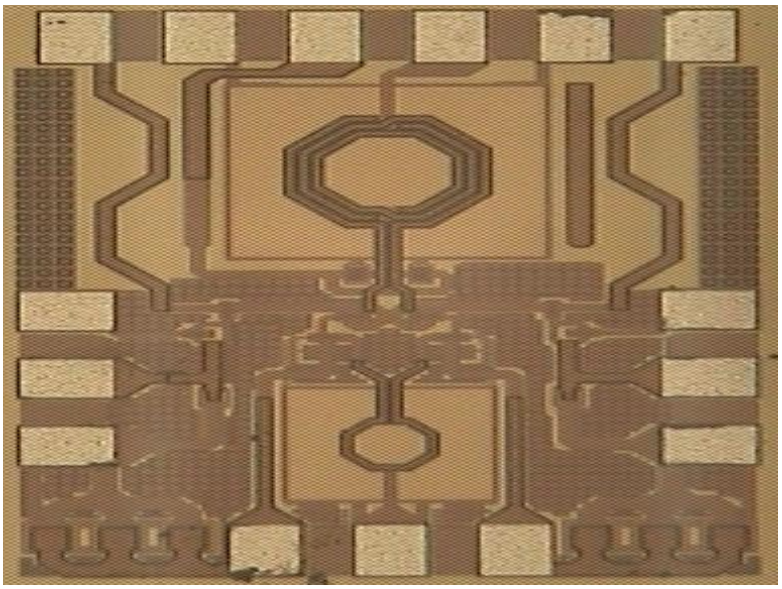

Figure 7. The photograph of the fabricated VCO chip (size: 0.499 mm²).

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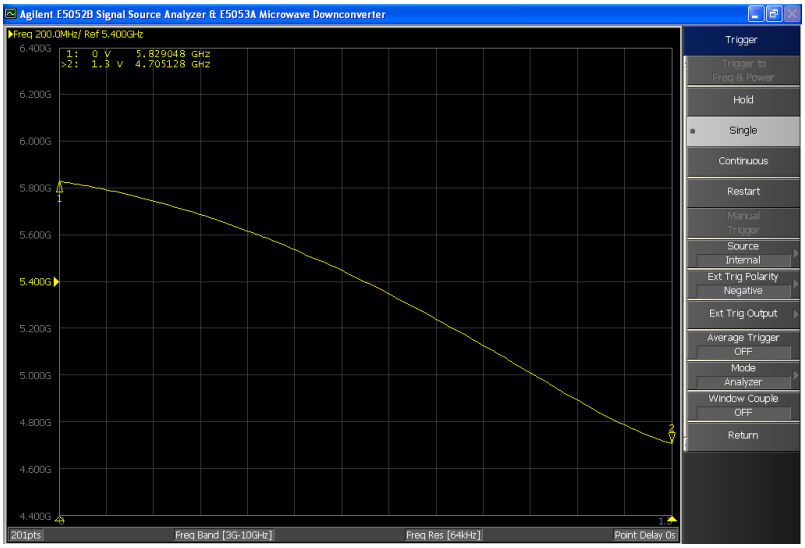

Figure 8. Measured tuning curve of the VCO.

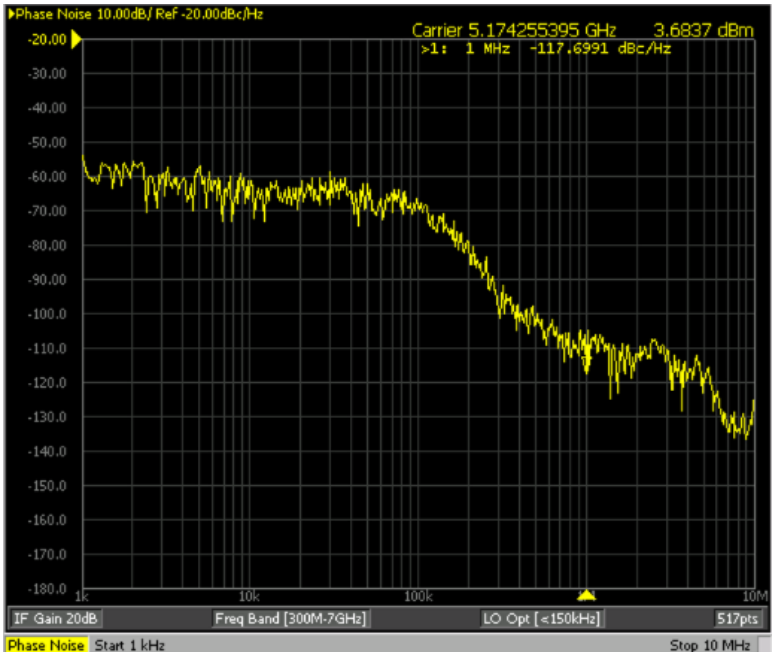

Figure 9. Measured phase noise at 1 MHz offset showing -117.69 dBc/Hz performance.

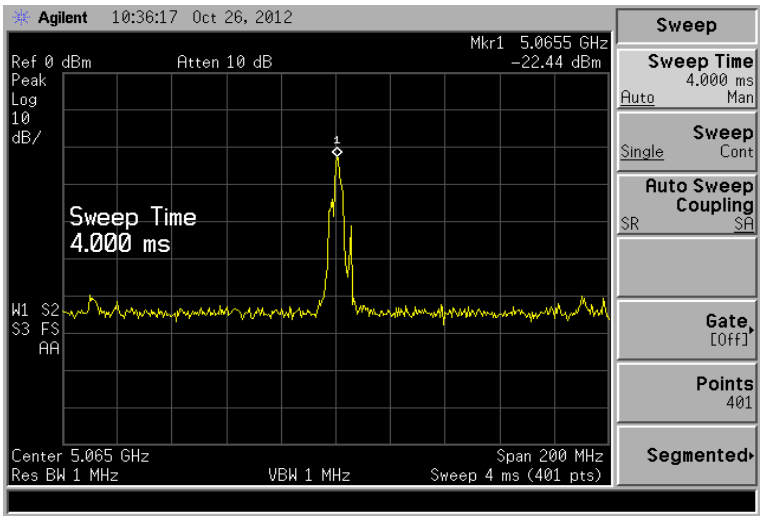

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Figure 10. Measured spectrum of the VCO at 5.065-GHz.

Table 1. Comparison between post-simulation and measured results of the proposed VCO.

	Post-simulation	Measurement
Frequency (GHz)	5	5.06
Tuning range (MHz)	1324	1124
Phase Noise (dBc/Hz)	-116.5	-117.69
FOM (dBc/Hz @MHz)	-181.4	-196.6
Output Power (dBm)	-4.6	-22.44
Power Consumption (mW)	8.1	3.4
Chip size (mm^2)	0.499	

Table 2. Performance comparison with other reported VCOs.

Ref.	CMOS Tech. (μm)	Frequency (GHz)	Phase Noise, dBc/Hz @1MHz	Tuning Range (%)	FOM (dBc/Hz)	P_{DC} (mW)	PFTN (dB)
[11]	0.18	5.3	-124	8	-190	13.5	-9.09
[14]	0.18	5	-122.7	6.4	-189.3	5.28	-8.25
[15]	0.18	5.2	-113.7	9.56	-180	9.7	N/A
[16]	0.13	5	-121	20	-189	4.2	N/A
This work	0.18	5.06	-117.7	22.2	-188.6	3.4	-4.3

4. Conclusions

In this work, a low-power, wide-tuning-range voltage-controlled oscillator (VCO) for C-band applications has been proposed and successfully implemented using the TSMC 0.18 μm 1P6M CMOS process. The design incorporates several techniques such as body-biasing and an optimized varactor structure to enhance tuning range and reduce power consumption, while maintaining low phase noise. The measured phase noise at a 1 MHz offset is as low as −117.6 dBc/Hz, and the achieved figure-of-merit (FOM) is −188.6 dBc/Hz. The VCO achieves a tuning range of 1124 MHz with a core power consumption of only 3.4 mW. These results demonstrate the proposed VCO's suitability for modern low-power communication systems, particularly in compact and battery-constrained IoT and 5G applications.

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Conflicts of Interest: The authors declare no conflicts of interest.

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